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A Design of Variable-Cutoff-Frequency CMOS High-Pass Filter using Low-Bias Current Control

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Abstract– **This paper presents a variable-cutoff-frequency CMOS high-pass filter, which is designed for low-power analog front-end applications. The filter employs a weak-inversion MOSFET network to synthesize a GΩ-range equivalent resistance, enabling low-frequency operation without relying on large on-chip resistors. The cutoff frequency is adjusted by a low-bias current control scheme consisting of four selectable 300 pA branches, which tune the effective equivalent resistance while maintaining minimal power consumption. A comparator utilizes a folded cascode stage for common-mode stabilization and accurate bias control. Implemented in a 180 nm CMOS technology, the proposed prototype occupies 0.0045 mm^2, consumes 0.749 μW, and provides five programmable high-pass corner frequencies ranging from 50 Hz to 100 kHz. The aforementioned features make the proposed architecture suitable for compact, energy-efficient front-end systems requiring reliable and tunable high-pass filtering.**

Keywords– **Variable-cutoff-frequency, CMOS, high-pass filter, low-power, analog front-end.**

1 Introduction

The demand for precise acquisition of low-frequency signals has intensified, thereby increasing the need for higher measurement reliability in analog front-end (AFE) systems [1–3]. In applications spanning biomedical systems and environmental monitoring, biosensors have become fundamental measurement interfaces. In the medical domain, biosensors provide rapid access to critical physiological information, enabling timely medical intervention and informing long-term treatment strategies [4, 5]. In scientific and environmental studies, biosensors deliver high-fidelity observations of biological and chemical variations, supporting investigations into physiological mechanisms, pollutant dynamics, and broader ecosystem behavior [6, 7]. These measurement capabilities underpin the development of advanced therapeutic technologies, diagnostic platforms, and environmental assessment systems, while providing reliable data for ongoing medical and environmental research. However, acquiring these signals is challenging because they are corrupted by low-frequency drift, electrode DC offsets, motion-induced signal changes, and other slow variations, which can significantly reduce the reliability of the measured signal [8, 9]. To fix these problems, a high-pass filter (HPF) is used to block low-frequency noise while keeping the useful signal content [10]. For systems operating in the sub-kilohertz or hertz range, the HPF must provide a very low and well-defined cutoff frequency. Achieving such cutoff frequencies typically requires GΩ-range resistance values. If implemented using conventional polysilicon resistors, these large resistances consume substantial silicon area [11] and have limited tunability. This constraint motivates the use of alternative high-resistance implementations suitable for compact and low-power integrated designs.

The design of the high-pass filter (HPF) using the CMOS technology proposed in this paper is built upon four selectable current branches, each with a fixed current value of 300 pA. The activation or deactivation of each current branch is selectively controlled through the corresponding digital control ($CTRL$) signal, thereby allowing the bias current for the resistor network operating in weak-inversion to be adjusted in discrete steps. The operating mechanism relies on the switching of these switches, which changes the total bias current in quantized increments. This controlled change directly modifies the value of the effective high-impedance resistor in the circuit, and consequently, the cutoff frequency of the high-pass filter is adjusted accordingly. Thanks to this switch-based approach, the circuit achieves programmable tuning while maintaining two important characteristics: low power consumption and a compact chip area. Additionally, a folded cascode amplifier (denoted as G_{m1}) is integrated to function as a bias-control comparator, playing a key role in stabilizing the common-mode voltage for the core of the high-pass filter, ensuring stable circuit operation across the entire tuning range.

HPF is employed in AFE to suppress power-line interference originating from the input supply, thereby preventing corruption of the measured signal. This brief presents an HPF that uses a MOS-based resistive network as the equivalent resistance, enabling area optimization and reduced power consumption while maintaining the targeted corner frequency. Designed in a 180 nm CMOS process, the circuit occupies a compact

area of 0.0045 mm^2, consumes 0.749 μW of total power, and features five programmable high-pass corners at 50 Hz, 1 kHz, 8.2 kHz, 50 kHz, and 100 kHz. These results confirm that the proposed design is suitable and efficient for low-power AFE systems requiring accurate, tunable, and area-efficient HPF.

2 System Architecture and Circuit Implementation

2.1 The proposed CMOS high-pass filter

Figure 1 shows the complete schematic of the proposed CMOS HPF, which utilizes a bias-control comparator circuit composed of a transconductance amplifier (G_{m1}) together with a source-follower circuit. The circuit operates as a RC filter consisting of a coupling capacitor (C_{in}) and an equivalent resistor (R_{in}) formed by a network of biased transistors. By decreasing the current flowing in the current mirror branch to the nA - μA range, the equivalent R_{in} value reaches the GΩ-scale. Therefore, the proposed filter achieves an extremely low cutoff frequency, defined by $f_c = 1/(2\pi R_{in}C_{in})$ [12]. In a traditional RC filter, achieving such a low cutoff frequency with standard polysilicon resistors would require a prohibitively large active area. To address this, the proposed design utilizes biased MOSFETs to implement the high resistance, which makes extension toward lower cutoff frequencies feasible in principle while preserving a compact active area.

In the cascode branch formed by *MN*1 and *MN*3-*MN*6, *MN*3-*MN*6 functions as a cascode device that shield the current source [13]. Particularly, *MN*3-*MN*6 are biased to maintain operation in the weak-inversion region, keeping a near constant voltage at nodes *Y* and *Z*. As a result, the V_{DS} of *MN*4-*MN*7 becomes nearly constant and matches that of *MN*2, ensuring that both transistor branches *MN*2 and *MN*4-*MN*7 operate with the same bias voltage. Since *MN*2 and *MN*4-*MN*7 have the same W/L ratios, they establish equal V_{GS}, resulting in more effective current replication from *MN*2 to *MN*4-*MN*7 compared to a conventional current mirror structure thus, $I_{bias} = I_{out1} = I_{out2}$.

In this work, R_{in} represents the equivalent input resistance mainly determined by bias current (I_{bias}), whereas C_{in} corresponds to the coupling capacitor at the input node. Since C_{in} is constant, the cutoff frequency is tuned by the bias current, which is achieved by controlling the total current flowing from the branches into transistors M_1 and M_2 through four selectable switches (*SW*1, *SW*2, *SW*3, *SW*4). When all four switches are turned on, the total current is given by

$$I_{bias} = I_0 + I_1 + I_2 + I_3 + I_4, \quad (1)$$

with each current branch carrying 300 pA. The output node V_{out} is then connected to the subsequent signal-processing block.

To simplify control over the four 300 pA bias branches, a 4-bit *CTRL* digital signal is applied to

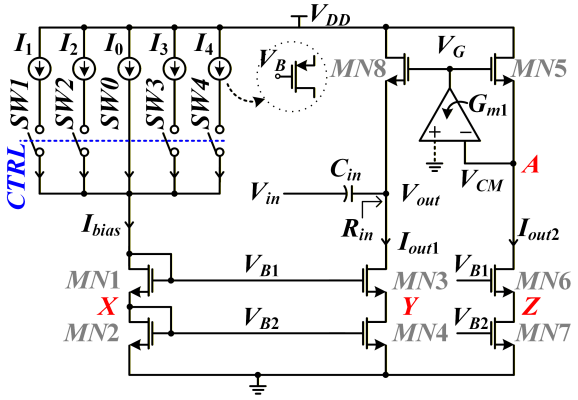

Figure 1. CMOS high-pass filter circuit.

*SW*1-*SW*4. When *CTRL* = 0000, 0001, 0011, 0111, or 1111, it enables the *SW*1 to *SW*4 branches, generating I_{bias} of 300, 900, 1200, 1500, and 1800 pA, respectively. By selectively activating various branches, the effective bias current may be modulated in discrete increments, allowing an adjustable compromise between cutoff frequency and power consumption. Each active branch functions in the weak inversion region to sustain GΩ-scale input resistance, while keeping the overall power consumption within the low-microwatt range.

2.2 Bias-control comparator circuit (G_{m1})

The schematic of the bias-control comparator, designed to provide high DC gain, wide bandwidth, and low-voltage operation for high-precision comparison, is shown in Figure 2. A folded-cascode architecture was adopted for G_{m1}. Compared to the conventional telescopic configuration, the folded cascode topology offers a significantly wider input common mode range (ICMR), which is critical for applications involving large signal swings. Furthermore, this architecture provides superior isolation between the input and output nodes, effectively mitigating the Miller effect and thereby enhancing the comparator's settling time. The proposed folded cascode circuit comprises a PMOS differential input pair driving an NMOS cascode load. The selection of a PMOS input stage not only minimizes flicker noise ($1/f_{noise}$) but also improves stability margins and enables an input range that extends down to the ground potential (GND).

The sizing of the CMOS transistors in G_{m1} and the source-follower circuit is shown in Table I. However, because of the limited open-loop gain of G_{m1}, the calibration loop cannot force node *A* to perfectly follow V_{CM}, giving rise to a systematic offset voltage defined as $\Delta V_{OS} = V_A - V_{CM}$ [14]. Moreover, $\Delta V_{OS} = V_A - V_{CM}$ increases due to device mismatches such as threshold-voltage variations, and leakage-current asymmetry at the comparison nodes.

The function of the transconductance amplifier (G_{m1}) is to generate the control voltage V_G of *MN*5 such that the common-mode potential at node *A* remains locked to V_{CM}. Because *MN*5 operates as a source-follower, any deviation of node *A* from V_{CM} is sensed and

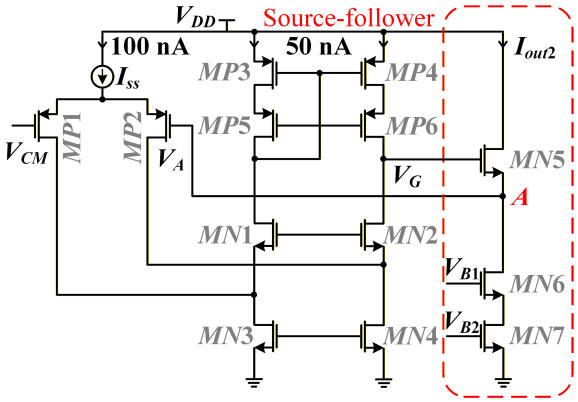

Figure 2. Comparator circuit.

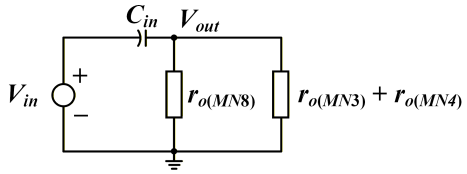

Figure 3. High-frequency equivalent circuit.

corrected through the feedback loop. If V_A rises above V_{CM}, G_{m1} reduces V_G, causing the source-follower $MN5$ to pull node A back toward the desired V_{CM} level.

Table I
Parameter of the comparator circuit

Parameter	W/L (μm)
$MP1$, $MP2$	15/0.7
$MP3$, $MP4$, $MP5$, $MP6$	7.5/0.7
$MN1$, $MN2$, $MN3$, $MN4$	8/0.7
$MN5$, $MN6$, $MN7$	10/0.4

2.3 Corner-frequency analysis of the proposed CMOS high-pass filter

Behavior of the circuit in Figure 1 is analyzed by replacing the transistor network around the output node with the small-signal equivalent shown in Figure 3. In this simplified representation, the output node is loaded by the parallel conductance, while the input signal is coupled through C_{in}.

The small-signal output resistance equivalent from Figure 1 is

$$r_{o(eq)} = \left(\frac{1}{r_{o(MN8)}} + \frac{1}{r_{o(MN3)} + r_{o(MN4)}} \right)^{-1}. \quad (2)$$

By using the relation $r_o = 1/g_s$, the equivalent resistance $r_{o(eq)}$ can be expressed in terms of conductance, yielding the total small-signal conductance

$$g_s = g_{s(MN8)} + g_{ds(MN3-MN4)}, \quad (3)$$

where, $g_{s(MN8)}$ is small-signal source conductance of transistor $MN8$, and $g_{ds(MN3-MN4)}$ is the small-signal drain-source conductance of transistors $MN3$-$MN4$ is given by

$$g_{ds(MN3-MN4)} = \frac{g_{s(MN3)} g_{s(MN4)}}{g_{s(MN3)} + g_{s(MN4)}}. \quad (4)$$

Applying KCL at the V_{out} node of the equivalent circuit yields the following time-domain relation

$$sC_{in} (V_{in} - V_{out}) = g_s V_{out}, \quad (5)$$

hence,

$$\frac{V_{out}}{V_{in}}(s) = \frac{s}{s + \frac{g_s}{C_{in}}}. \quad (6)$$

Equation (6) indicates that the proposed circuit is a first-order active high-pass filter. Accordingly, the asymptotic transition-region slope is 20 dB/decade. The CTRL signal changes the effective bias current and shifts the cutoff frequency, while the filter order and overall response shape remain unchanged. From the pole of the transfer function, the cutoff frequency is obtained as

$$f_c = \frac{g_s}{2\pi C_{in}}. \quad (7)$$

From (7), for a fixed Cin, the cutoff frequency is directly proportional to the effective conductance gs. Therefore, reducing fc from 50 Hz to 0.1 Hz would require an approximately 500× reduction in gs. In principle, this can be achieved by further reducing the bias current and/or increasing the effective RC time constant. However, in the ultra-low-current regime, the achievable cutoff becomes increasingly sensitive to leakage, mismatch, and PVT variation. The forward diffusion current in weak inversion of $MN8$ is

$$I_F = K_W \beta U_T^2 e^{\frac{V_P - V_S}{U_T}}, \quad (8)$$

where depends only on the potential difference $V_P - V_S$. The reverse diffusion current through $MN3$-$MN4$ is given by

$$I_R = K_W \beta U_T^2 e^{\frac{V_P - V_D}{U_T}}, \quad (9)$$

The constant $K_W = 2n$ incorporates the subthreshold slope factor n, $\beta = \mu_n C_{ox}(W/L)$. The thermal voltage is given by $U_T = kT/q$. The pinch-off potential V_P varies approximately linearly with the gate voltage and can be expressed as $V_P \cong (V_G - V_{TH})/n(V_G)$, with $n(V_G)$ represents the slope factor, which in this case, depends on the gate voltage V_G [15]. With these definitions, the small-signal source conductance of $MN8$ becomes

$$g_{s(MN8)} = \frac{\partial I_F}{\partial (V_P - V_S)} \cong K_W \beta U_T e^{\frac{V_P - V_S}{U_T}}, \quad (10)$$

The conductance of transistors $MN3$-$MN4$ is obtained from the derivative of the reverse diffusion current with respect to $(V_P - V_D)$, i.e., $g_{ds} = \partial I_R / \partial (V_P - V_D)$. Using (4), the small-signal drain–source conductance becomes

$$g_{ds(MN3-MN4)} \cong K_W \beta U_T \frac{e^{\frac{V_{P3} - V_{D3}}{U_T}}}{e^{\frac{\Delta V}{U_T}} + 1}, \quad (11)$$

where, ΔV is defined as $(V_{P,MN3} - V_{D,MN3}) - (V_{P,MN4} - V_{D,MN4})$.

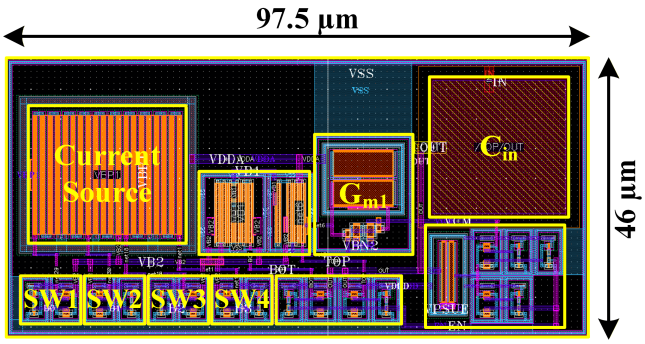

Figure 4. Layout of the proposed CMOS HPF.

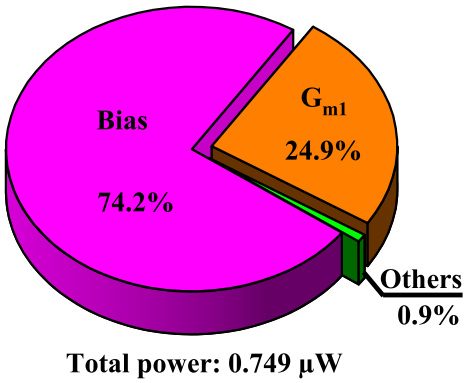

Figure 5. Total power consumption.

2.4 Simulation results and discussion

Figure 4 shows the layout of the proposed CMOS HPF with the comparator circuit. Using the 180 nm CMOS process, the circuit design occupies an area of 97.5 μm $\times$ 46 μm, corresponding to approximately 0.0045 mm^2. All simulations are performed under a 1.8 V supply, with the common-mode reference (V_{CM}) set to 900 mV and an input coupling capacitor C_{in} = 500 fF. As illustrated in Figure 5, the proposed design consumes 0.749 μW in total, with the bias-control comparator (G_{m1}) accounting for 24.9% of the total power budget.

The bias current (I_{bias}) is generated from five parallel 300 pA branches, each enabled through the 4-bit CTRL digital signal. With the *CTRL* settings 0000, 0001, 0011, 0111, and 1111, the circuit generates bias currents of 300 pA, 900 pA, 1200 pA, 1500 pA, and 1800 pA, respectively. These discrete current levels modify the equivalent resistance and, consequently, shift the high-pass cutoff frequency. These five bias settings produce the five resulting frequency responses shown in Figure 6, with corresponding cutoff frequencies of approximately 50 Hz, 1 kHz, 8.2 kHz, 50 kHz, and 100 kHz.

Figure 7 demonstrates the corner-dependent frequency response of the proposed high-pass filter under *CTRL* = 0001, V_{DD} = 1.8 V, and a temperature of 27 °C. The cutoff frequency exhibits noticeable variation across FF, FS, SF, SS, and TT corners, ranging from 647.4 to 4.25 kHz. The FF corner exhibits the highest cutoff frequency because higher carrier mobility makes the transistors more responsive, allowing them

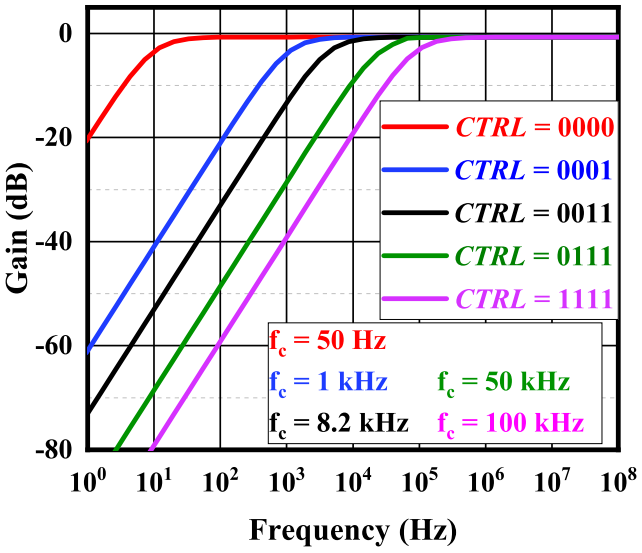

Figure 6. Simulated frequency responses for different CTRL settings.

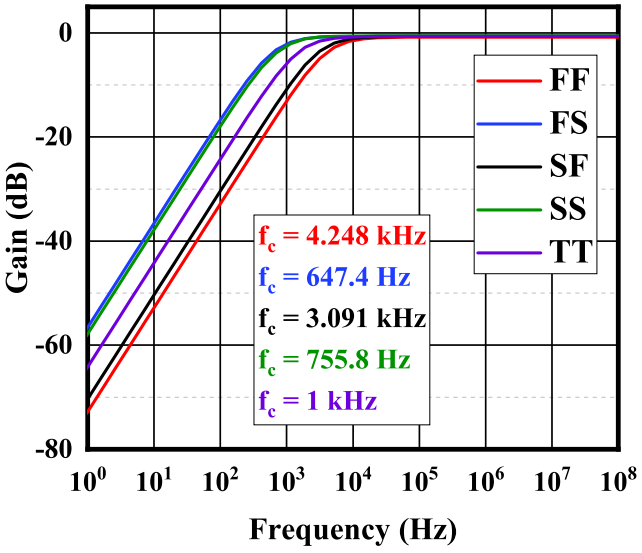

Figure 7. Simulated corner frequency responses.

to conduct more effectively even in the weak inversion region, leading to a higher cutoff frequency. In contrast, the SS corner produces the lowest cutoff frequency since the reduced mobility weakens the conduction capability of the devices.

Despite these shifts, the overall high-pass characteristic is preserved across all corners, confirming that the filter maintains stable functional behavior under process variations. These results highlight the importance of accurate bias-current control to ensure predictable corner-frequency settings in practical implementations. Although the cutoff frequency shows a relatively large spread across process corners, the gain and stability margins remain within a narrow range. Therefore, the main effect of process variation is reduced cutoff-frequency accuracy rather than loss of filter stability.

The corner simulation results summarized in Table II with *CTRL* = 0001 confirm that the electrical behavior

of the proposed G_{m1} varies noticeably across FF, SS, FS, SF, and TT corners. Significant shifts are observed in gain-bandwidth and common-mode rejection, together with large variations in the cutoff frequency and the total bias current. These results highlight that the weak-inversion operation of the circuit is highly sensitive to process conditions and therefore requires proper control of the bias current to maintain consistent performance. Such tuning is essential for ensuring the stable operation of the proposed CMOS HPF and for achieving a process-aware signal conditioning chain in practical implementations.

Table II
CORNER SIMULATION RESULTS (V_{DD} = 1.8 V, T = 27 °C, $CTRL$ = 0001)

Para.	FF	SS	FS	SF	TT
Gain (dB)	79.81	81.66	81.14	80.33	80.78
GBW (MHz)	14.25	6.65	7.315	12.96	9.77
PM (°C)	55	51	52	49	50
GM (dB)	73.71	73.81	72.47	71.78	72.73
Cutoff freq. (Hz)	4.25k	755.8	647.4	3.09k	1k
Current (nA)	644.77	261.22	278.78	586.83	413.7
Power (μW)	1.16	0.47	0.25	1.06	0.75

Figure 8 presents the open-loop response of G_{m1}, where the DC gain reaches approximately 80.7 dB. The simulated gain-bandwidth product is about 9.7 MHz, confirming that the transconductor provides adequate loop gain over a relatively wide frequency range. The phase margin of approximately 50°C further indicates a stable feedback loop without any oscillatory tendencies. These characteristics demonstrate that G_{m1} achieves robust small-signal stability under the intended operating conditions.

Monte Carlo simulation results for 200 samples are presented in Figure 9, illustrating the statistical spread of the DC gain and phase characteristics of the proposed G_{m1} circuit. As shown in Figure 9(a), the DC gain exhibits a tightly clustered distribution with a mean value of approximately 80.7 dB and a small standard deviation of 257 mV-equivalent, indicating strong robustness against device mismatch. Similarly, Figure 9(b) shows the phase margin centered around 50.036°C with a standard deviation of 245 mV equivalent, confirming that the stability margin remains consistent across mismatch variations. These results demonstrate that the proposed weak-inversion biasing and current-replication scheme maintain stable small-signal performance under statistical variations, ensuring reliable operation in practical implementations.

Table III summarizes the performance of the proposed CMOS HPF, compared with the state-of-the-art [11], [14], and [16]. Although prior works mainly target sub-Hz to low-frequency high-pass filtering for slow biosignal recording, the proposed

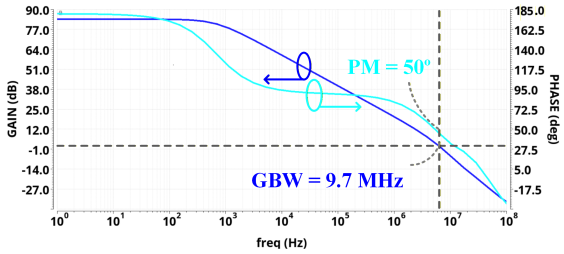

Figure 8. Open-loop frequency response of G_{m1}.

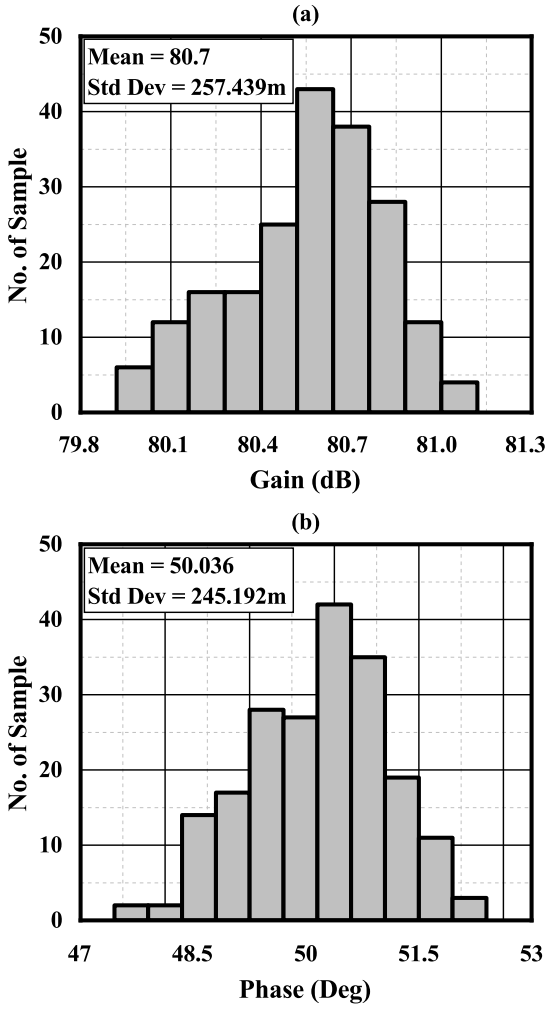

Figure 9. Monte Carlo simulation results over 200 runs. (a) DC gain, (b) Phase margin.

architecture demonstrates a higher cutoff frequency range (50 Hz - 100 kHz) in this implementation while still being inherently compatible with sub-Hz operation through further bias-current scaling. Despite operating at a higher corner frequency in the present implemented, the circuit maintains a low power consumption of 0.749 μW and a compact silicon area. Additionally, it provides discrete tunability that is not available in [14] and [16]. This indicates that the architecture is flexible and can be extended toward sub-Hz applications without causing any significant impact on power consumption or area efficiency.

Table III
Performance comparison with prior works.

	[11]	[14]	[16]	**This work**
Technology (μm)	0.35	0.35	0.18	**0.18**
Filter topology	HPF	HPF	LPF	**HPF**
Supply voltage (V)	2	1.5	3.3	**1.8**
Filter order	2	1	2	**1**
Cutoff frequency (Hz)	38-200	0.1	500	**50-100k**
Tunable cutoff	Yes	No	No	**Yes**
Power consumption (μW)	1.24	1.05	2.484	**0.749**

3 Conclusion

This work presents a compact, low-power high-pass filter that uses a weak-inversion MOS resistance network together with four 300 pA current branches, which are enabled by switches controlled through the CTRL digital signal. Implemented in a 180 nm CMOS process, the design occupies only 0.0045 mm^2, consumes 0.749 μW, and provides five programmable cutoff frequencies from 50 Hz to 100 kHz. The switch-configurable bias current enables stable corner tuning while sustaining GΩ resistance levels. The architecture also supports further bias scaling, allowing extension toward lower cutoff frequencies without significantly affecting power or area, making it well-suited for flexible AFE integration.

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