Regular Article

Design of a Configurable 4-Channel Analog Front-End for EEG Signal Acquisition on 180nm CMOS Process

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Abstract– **In this work, a 4-channel Analog Front-End (AFE) circuit has been proposed for EEG signal recording. For EEG recording systems, the AFE may handle a wide range of sensor inputs with high input impedance, adjustable gain, low noise, and wide bandwidth. The buffer or current-to-voltage converter block (BCV), which can be set to operate as a buffer or a current-to-voltage converter circuit, is positioned between the electrode and the main amplifier stages of the AFE to achieve high input impedance and work with sensor signal types. A chopper capacitively-coupled instrumentation amplifier (CCIA) is positioned after the BCV as the main amplifier stage of the AFE to reduce input-referred noise and balance the impedance of the overall AFE system. A programmable gain amplifier (PGA) is the third stage of the AFE that allows the overall gain of the AFE to be adjusted. The suggested AFE operates in a wide frequency range of 0.5 Hz to 2 kHz with a high input impedance bigger than 2 TΩ, and it is constructed and simulated using a 180nm CMOS process. With the lowest 100 dB CMRR and low input-referred noise of 1.8 µVrms, the AFE can achieve low noise efficiency. The design incorporates new features such as the BCV to enhance input variety, and the IRN and CMRR coefficients exhibit notable enhancements in comparison to prior research. EEG signals can be acquired with this AFE system, which is very useful for detecting epilepsy and seizures.**

Keywords– **Analog front-end, EEG signal acquisition, low noise, high input impedance, 4-channel, 180nm CMOS process.**

1 Introduction

Currently, integrated circuit research and applications in the biomedical field are receiving a lot of attention. The development of CMOS technology and analog design methodologies has contributed to the efficiency and necessity of biomedical signal acquisition, particularly for EEG signals. The purpose of this work is to develop a 4-channel configurable Analog Front-End (AFE) circuit that can receive and preprocess Electroencephalogram (EEG) signals from a variety of current and voltage sensors with extremely small voltage or current amplitudes. To make pre-processing easier, the EEG signal sources from the electrodes in Figure 1 will be enhanced. An electrophysiological technique called EEG is used to record electrical activity in the brain. This sort of signal has been widely used in the medical industry, particularly in the field of neurology [1–3]. The EEG signal has a very low frequency range (0.5-100 Hz) and an average amplitude (3-100 µV). Furthermore, it is made up of multiple subband signal components with the following operating frequencies: Delta (δ: 0.5-4 Hz), Theta (θ: 4-7 Hz), Alpha (α: 8-12 Hz), Beta (β: 13-30 Hz), and Gamma (γ: 30-100 Hz) [4–7]. Additionally, the impedance at the sensor's output is crucial in boosting the EEG signal's amplitude and reducing noise on the transmission path. It emerges between the skin and the electrode (wet or dry). The authors of research [8] reported that the sensor's output impedance was quite high within the EEG signal's bandwidth. The impedance may vary from 87 KΩ-1 MΩ, and at 1 Hz, it may even exceed 1 GΩ.

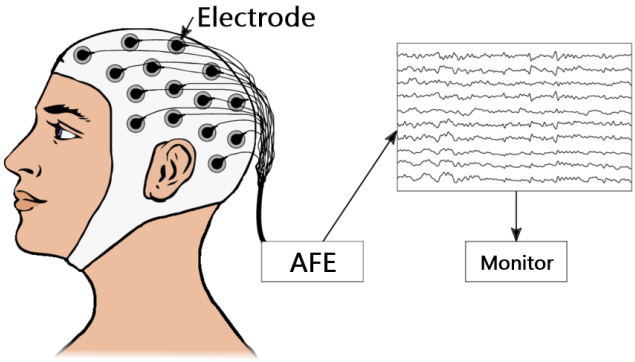

Figure 1. EEG signal measurement with electrodes.

The acquisition of brain signals has emerged as a potential therapy for brain illnesses such as epilepsy and convulsions. Feedback stimulation is required for the effective treatment of brain illnesses. By employing signal processing techniques, the brain's EEG signals are obtained and processed in this therapy procedure to rewrite the stimulation waveform. The concept is derived from earlier studies on the architecture of AFEs with one or more input channels. The signal from the

EEG sensor, which contained a lot of noise, was amplified to different levels by the AFE design in [9] using a Low Noise Amplifier block (LNA) and a Programmable Gain Amplifier block (PGA) to make it visible. Thermal noise and flicker noise are two types of common noise detected in the recording of EEG signals at low frequencies. They commonly occur in circuits without filter components. In addition, another study [10] showed how the AFE's structure functions over an enormous frequency range of 0.1 Hz to 10 kHz when paired with the Analog-to-Digital Converter (ADC) at the back. Similarly, this approach demonstrated the adaptability of signal analysis for humans and computers. A low-noise design with tiny EEG signal amplitudes ($\leq$10 µV) was suggested by the very significant input-referred noise (IRN) value of 2.68 µVrms from 0.1 Hz to 10 kHz. Numerous applications, such as brain-computer interfaces (BCIs) and the prediction of epileptic seizures, showed success with this approach.

Based on previous research, the authors conclude that the design of these AFE circuits primarily recorded EEG data at the voltage-type sensor output and that their ability to suppress low-frequency noise is not excellent. In fact, electronic sensors can provide many type of output signals including voltage, current, capacitance, resistance, and so on [11, 12]. The AFE system, on the other hand, only handles one or two types of sensor output signals. As a result, a Buffer or Current-To-Voltage Converter (BCV) is needed to setup the input, which comprises voltage type or current type. This research developed a 4-channel AFE system from our paper presented at the conference ATC 2023 that can record EEG signals from a variety of brain electrodes. The main contributions of the proposed AFE circuit consist of low noise, high input impedance, flicker noise efficiency, configurable input signal type, and configurable gain levels.

The remaining part of the paper's structure is as follows: The operational concept and architecture of the circuit are discussed in Section 2. The experimental results are presented in Section 3. Section 4 brings the paper to a conclusion.

2 Circuit Architecture

2.1 Architecture Overview of 1-Channel AFE

The proposed 1-channel AFE circuit, depicted in Figure 2, consists of the following blocks:

- BCV (Buffer or Current-to-Voltage Converter).
- CCIA (Coupled-Capacitive Instrument Amplifier).
- PGA (Programmable Gain Amplifier).
- Supplementary blocks: Ring Oscillator, Internal bias.

As seen in Figure 2, the three major circuits that make up the 1-channel AFE system are the BCV, CCIA, and PGA. This circuit's input signal, regardless of its voltage or current type, passes through the BCV circuit. The BCV's output then keeps going across the CCIA and PGA. The PGA's output will be connected to the AFE system's final output. As a result of the BCV circuit's

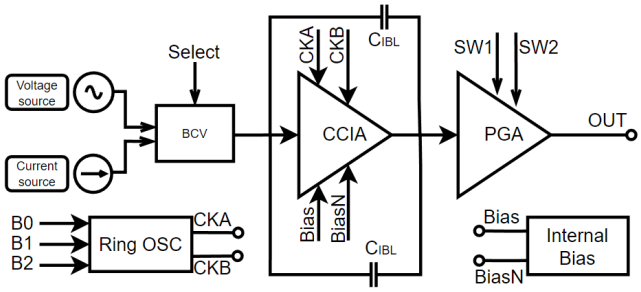

Figure 2. Block diagram of 1-channel AFE.

increased input impedance, the signal passes through the CCIA circuit, which reduces noise and amplifies the incredibly weak input signal. The output signal from the CCIA circuit will be forwarded to the PGA circuit in order to boost the amplitude of the input signal. A pair of C_{IBL} capacitors are located at the CCIA's output feedback into the input to enhance the input impedance. This approach also reduces the effect of noise at the sensor's output. Two changeable pins (SW) on the PGA circuit will help the amplitude of the output signal boost with various gain levels.

2.2 Buffer or Current-to-Voltage Converter (BCV)

The authors established the BCV circuit architecture to be compatible with various kinds of EEG sensors (current or voltage sensors). This circuit can select amongst input signals by setting a "Select" bit high (1 V) or low (0 V). The circuit is built as illustrated in Figure 3.

The brain tissue and electrode interaction causes a large impedance mismatch at the AFE's input when the EEG signal is being measured at the sensors or electrodes [13–16]. In order to improve EEG signal acquisition, the input impedance of AFE may occasionally be as high as 1 GΩ [17–20]. As a result, managing the electrode-tissue impedance mismatch requires a high input impedance (more than 1 GΩ) for the BCV at the first AFE stage. To guarantee the input impedance magnitude, the BCV circuit architecture includes active components like Op-Amp. The low amplitude signal that crosses the CCIA and PGA blocks is amplified as effectively as possible based on this method. The BCV circuit's architecture necessitates the use of multiple 2-stage Op-Amps as it will be driving large loads (like the PGA and CCIA) behind it. Figure 4 displays the 2-stage Op-Amp schematic. The multiplexer (MUX) 2-1 circuit will be used to select the signal that corresponds to the current or voltage source of the sensor as the BCV input. Table I presents this selection.

Table I
Function of the BCV as Buffer or I-V Converter

Select Pin	Input	Types of Circuit
High (1 V)	Voltage source	Buffer
Low (0 V)	Current source	I-V Converter

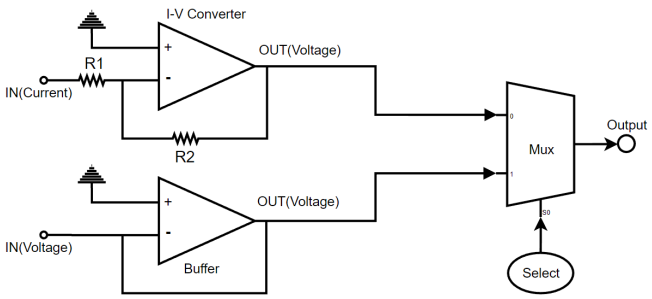

Figure 3. Buffer or Current-to-Voltage Converter Block.

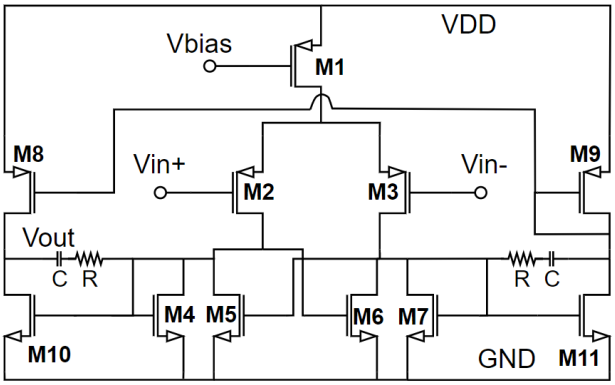

Figure 4. The schematic of the 2-stage Op-Amp circuit.

2.3 Capacitively–Coupled Instrumentation Amplifier (CCIA)

Biomedical electronics circuits usually use the CCIA circuit because of its low noise and ability to remove common mode DC input. Flicker noise is a crucial consideration for circuits operating at low frequencies, especially biomedical electronic circuits [21, 22]. Flicker noise in semiconductors is presented at both the substrate layer and the oxide gate [23]. Currents may be randomly discharged as flicker noise after being locked in an energy state while passing through this layer. Op-Amp circuits that are placed before the CCIA block, like the BCV block, may experience this flicker noise. As a result, the approach is to modulate the EEG signal from low to high frequency using circuit Chopper 1. After that, the high-frequency signal is amplified to a particular amount. Finally, before delivering the signal to the CCIA output, Chopper 2 demodulates the high-frequency and larger amplitude signal to a low-frequency signal. In addition, a high-pass filter circuit is built by connecting the resistor R_f and capacitor C_f to reduce undesirable low-frequency noise [24–26]. Moreover, the DSL (DC servo loop) block is used to reduce the DC offset at the sensor, supporting the CCIA circuit in avoiding the saturation voltage threshold at the output [27, 28]. Figure 5 depicts the CCIA circuit.

2.4 Programable Gain Amplifier (PGA)

Gain control is a characteristic of PGA circuit design [29–31]. This will allow the AFE circuit to alter the gain factor, allowing users to amplify input signals of varying amplitudes. Using an Op-Amp circuit and capacitor arrays, the PGA circuit amplifies the signal

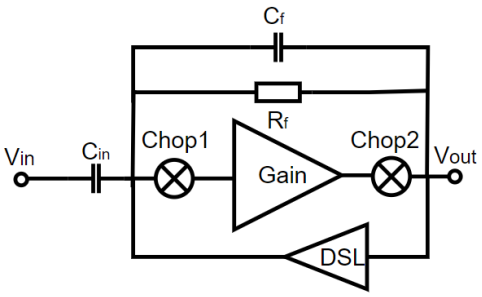

Figure 5. The CCIA circuit schematic.

from the previous CCIA block. Two switches (SW1 and SW2) control the equivalent feedback capacitance. The PGA circuit generates an adjustable gain based on the configuration of the two switches. The PGA circuit diagram is shown in Figure 6.

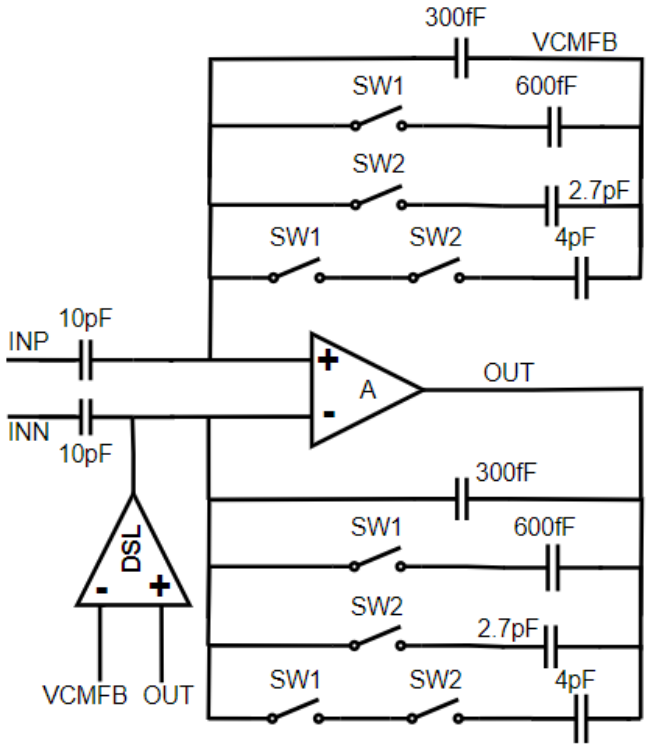

Figure 6. The PGA circuit schematic.

2.5 Internal Bias

The term "Bias" relates to the selection of basic operating conditions for an electrical circuit. Current and voltage are two examples of operational conditions. Internal current and voltage must be stable in order for a circuit to work effectively. The current and voltage readings are now known as "Bias" values.

The Internal Bias block is depicted in Figure 7. In this design, the Internal Bias block will create two stable voltage levels to supply the circuits at lower levels within. The fundamental reason for bias voltage is that the AFE circuit includes a variety of amplifiers that perform well with a specific bias.

Figure 8 depicts the Internal Bias schematic for this study. The circuit generates Bias voltage = 658 mV and

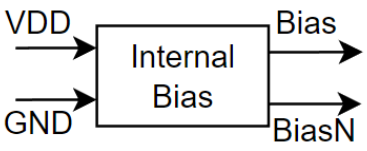

Figure 7. Block diagram of Internal Bias.

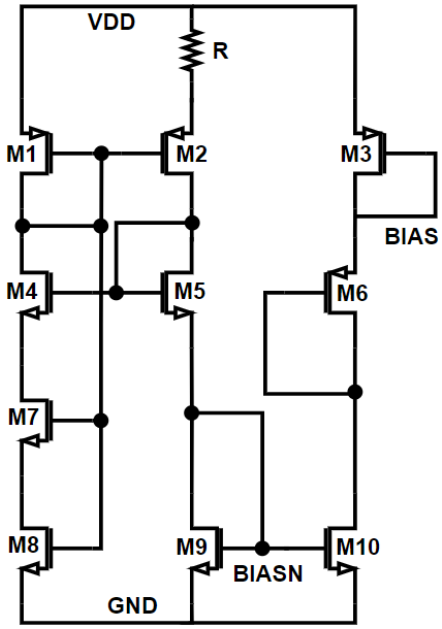

Figure 8. Internal Bias circuit schematic.

BiasN voltage = 286 mV with supply power: VDD = 1 V and GND = 0 V. To obtain the required voltage levels, the authors use a voltage divider structure through resistors or the diode-connected load structure. When a certain resistor value cannot be designed due to layout constraints, the diode-connected load structure is used.

2.6 Ring Oscillator

The Ring Oscillator's function is to produce a clock pulse, which is a periodic electrical signal. The signal that is generated will have a square waveform. Simple ring oscillator structures only require an odd number of serial inverters; the ring oscillator circuit in Figure 9 has three odd-numbered inverter circuits. Three bits–B0, B1, and B2–control the Ring Oscillator's output signal frequency.

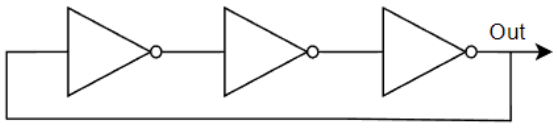

Figure 9. Odd-Inverter's Ring Oscillator circuit schematic.

The circuit comprises three bits (B0, B1, B2) that control the output frequency of the Ring Oscillator, as shown in Figure 10. These output signals of different frequency values will be fed into the two Chopper circuits of the CCIA block described above. The Ring Oscillator block will be made up of three delay-generating blocks (Delay Cell) connected in series to create the appropriate frequency difference. Furthermore, the circuit contains two Flip-Flop D (FFD) components that divide the frequency by four. Figure 11 depicts a frequency divider circuit employing FFD with the desired frequency value of several tens of thousands of Hz at the output. After passing through two FFDs, the signal will be routed through two inverter arrays to consolidate its ability to drive loads. The first array is the CKB pin, which is subsequently connected to the CKA pin via the second array. In actuality, the CKA and CKB output signals have the same frequency but phase inversion.

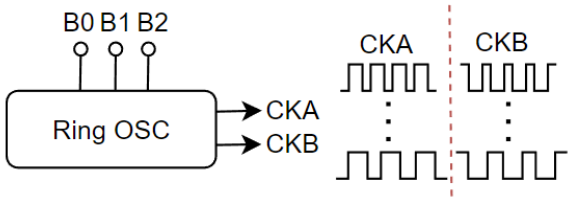

Figure 10. The output signal frequency of the Ring Oscillator.

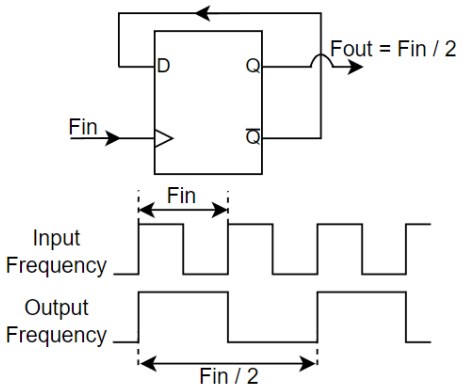

Figure 11. Flip-Flop D circuit for frequency division.

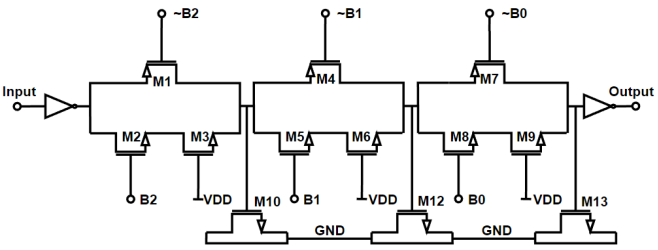

Figure 12. Delay cell circuit schematic.

The Delay Cell block is made up of two inverters that are inserted at the start and end of a Voltage-controlled Oscillator (VCO) circuit to generate a particular delay. Furthermore, the VCO block has three stages that establish the delay in the time domain. As shown in Figure 12, each stage is a Transmission Gate (TG), which includes two NMOS and one PMOS transistor connected in parallel. Because TG is controlled by a couple of external voltages, it can change the delay value based on the capacitances behind it [32]. Figure 13 depicts the FFD schematic. Figure 14 shows

the whole structure of the Ring Oscillator circuit, which comprises circuits such as the Delay Cell, Flip-Flop D, and Inverter.

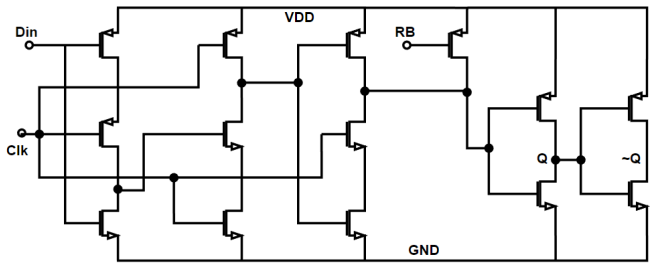

Figure 13. Flip-Flop D circuit schematic.

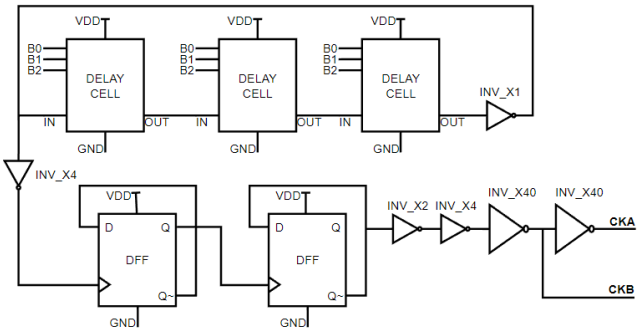

Figure 14. The structure of the Ring Oscillator circuit.

2.7 Design of 4-Channel Analog Front-End Circuit

The proposed 4-channel Analog Front-end (AFE) system is shown in Figure 15. The design includes 4 blocks of a 1-channel AFE circuit. We utilize two reference buffers as the negative input, so each of them shares with two 1-channel AFE circuits in order to accomplish the goal of saving area and resources as illustrated in Figure 16. Additionally, to reduce the system's overall power consumption, the 4-channel AFE circuit employs the same Internal Bias and Ring Oscillator circuit. The addition of the BCV block makes it simple to select an input from a variety of sensor output signal types (current and voltage). In order to prevent the effects of the impedance mismatch of the AFE system caused by brain tissue and electrodes, BCV can be configured as a buffer or a current-to-voltage converter using two Op-Amps to achieve high input impedance. A good way to both reduce flicker noise and stimulate input signal is to use the PGA and CCIA together. For the purpose of recording EEG signals, the CCIA functions as the first-stage amplifier. The input signal is low noise with the CCIA, and the DC offset voltage that directly affects the signal from the sensor is completely eliminated. The CMRR and IRN factors are thus significantly reinforced. Meanwhile, the PGA acts as the second-stage amplifier, increasing the overall gain of the AFE with four different levels. The amplitude of the output signal can be changed by controlling the expected gain values with two PGA circuit switches. Based on the 180nm CMOS process, the structure of a configurable low-noise 4-channel AFE was designed.

3 Experimental Results

3.1 Buffer or Current-to-Voltage Converter Circuit

As previously stated, the BCV circuit is made up of two basic blocks: a current-to-voltage converter and a buffer. In order to test the BCV circuit, we need to provide an input signal with an amplitude of 50 µV for voltage and -5 µA for current, respectively, with the frequency of 1 kHz in the time domain. Next, with the goal to assess how well the circuit is working, we will look at the signal at the BCV circuit's output. The current and voltage sources that will be fed into the BCV circuit are depicted in Figure 17. The output waveform displayed in Figure 18 of the BCV further ensures that the type of signal after conversion is voltage with an estimated amplitude of 50 µV.

To evaluate the performance of this circuit, the AFE's input impedance is simulated. Figure 19 depicts the input impedance result. This circuit has a relatively high input impedance (>2 TΩ), making it appropriate for the sensor impedance requirement and low-noise capability.

3.2 Internal Bias

The simulation waveform based on the DC and transient simulation is shown in Figure 20 and Figure 21 with the VDD of 1 V and the VSS of 0 V as follows. According to the results of the previous two simulations, the circuit performed as expected.

3.3 Ring Oscillator

The above circuit generates frequencies using three bits (B2, B1, B0): 000, 001, 010, 011, 100, 101, 110, and 111 with the voltage supply of the VDD of 1 V and the VSS of 0 V. The frequency results at the CKA pin are measured at the pre-layout and post-layout simulation shown in Table II. The same frequencies are achieved at the CKB pin.

Table II
The Frequency Results with 3-bit Settings

Bit (B2 B1 B0)	Pre-Layout (kHz)	Post-Layout (kHz)
000	28.35	28.17
001	24.8	24.75
010	21.76	21.79
011	19.61	19.61
100	18.27	18.25
101	16.73	16.64
110	15.23	15.29
111	14.14	13.99

3.4 The Proposed AFE Circuit

The 4-channel AFE circuit is built from four 1-channel AFE circuits. As a result, the simulation will be run on each 1-channel AFE circuit. The BCV, CCIA, and PGA blocks make up the 1-channel AFE circuit. The input signal to the circuit can be either a current or a voltage

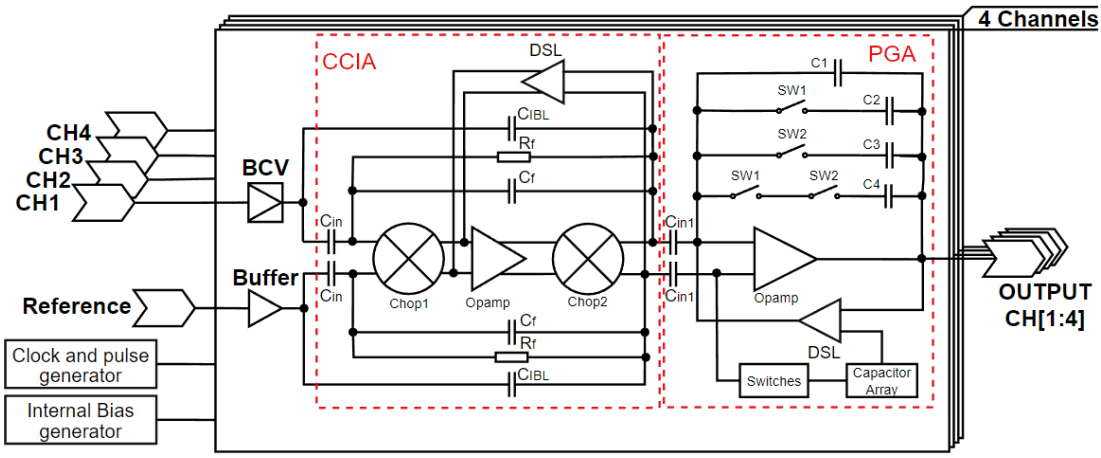

Figure 15. The architecture of the proposed configurable 4-channel AFE.

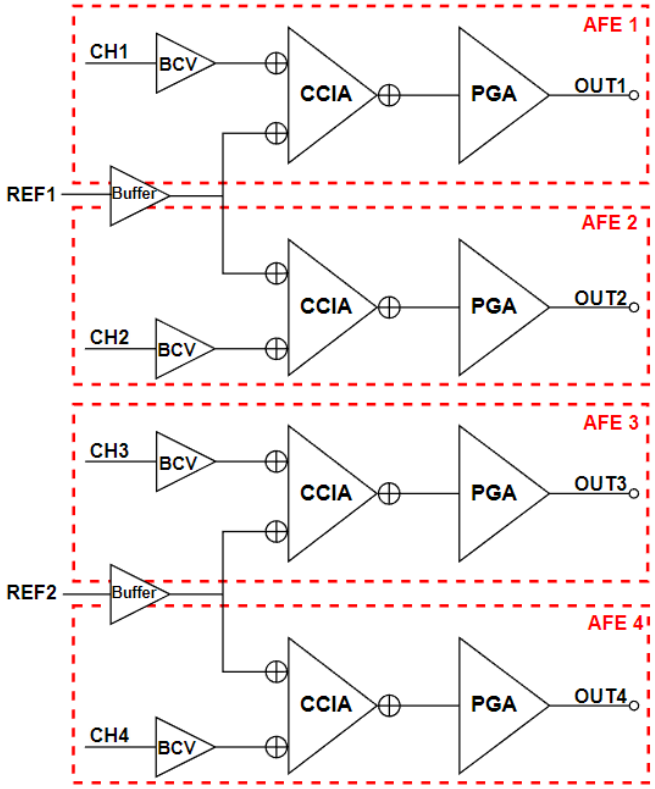

Figure 16. Block diagram of the 4-channel AFE sharing reference input signals.

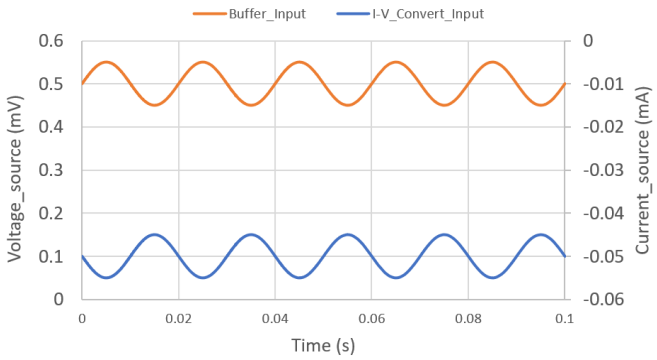

Figure 17. The current and voltage input signals of the BCV circuit.

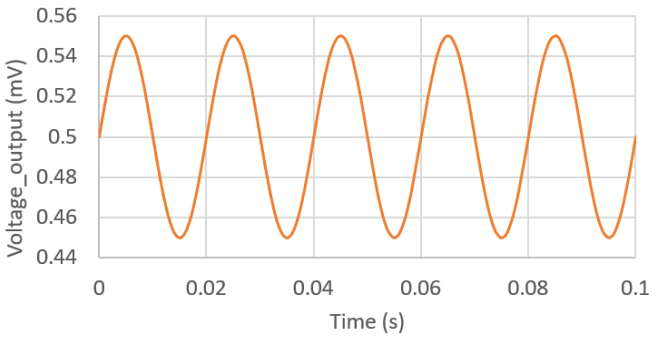

Figure 18. The output voltage signal of the BCV circuit.

source. The user has to control the "Select" bit of the BCV block, as shown in Table I, to select the type of input signal. The signal is then processed by the CCIA circuit, which filters noise and amplifies it to the desired level. By passing it through the PGA circuit, the signal is amplified once more. The two switches (SW1 and SW2) are used to configure the gain in the PGA circuit. The AFE circuit's output port corresponds to the PGA circuit's output port. The overall gain of the 1-channel AFE circuit can be calculated by measuring the value at this pin.

3.4.1 AC Simulation: The gain simulated at the AFE's output ranges from 42 dB to 70 dB for an input waveform with Magnitude = 1 V, as shown in Figure 22. Furthermore, the input-referred noise (IRN) and common-mode ratio rejection (CMRR) values are measured to evaluate the performance of the circuit depicted in Figure 23. The technique and approach for creating the testbench for evaluating the circuit using IRN and CMRR values are described in [33] and [34], respectively.

3.4.2 Transient Simulation: The input signal parameters include an amplitude of 50 µV and a frequency of 1 kHz. Figure 24 shows the output waveform produced by this input signal. SW1 and SW2 are configured as follows: 00, 10, 01, 11. Each bit pair will correspond to a different output amplitude. The circuit operates properly between 0.5 Hz and 2 kHz.

The layout for the 4-channel AFE circuit based on the

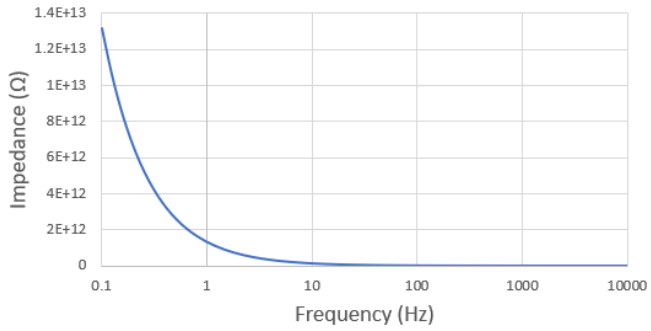

Figure 19. The input impedance of Op-Amp.

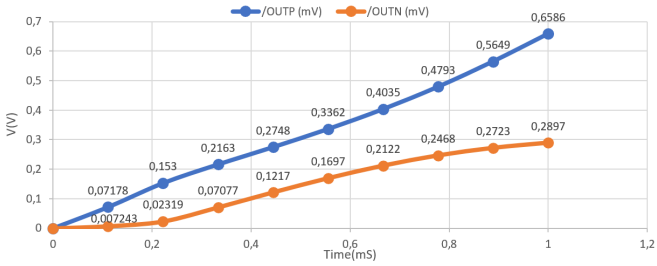

Figure 20. The DC simulation result of Internal Bias circuit.

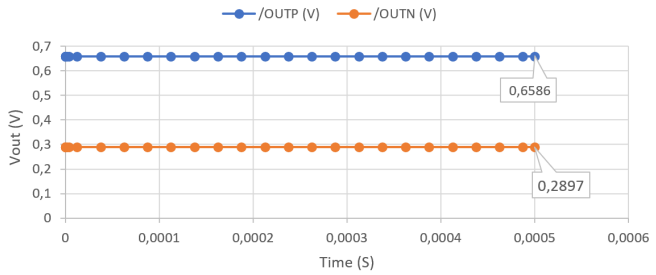

Figure 21. The transient simulation result of Internal Bias circuit.

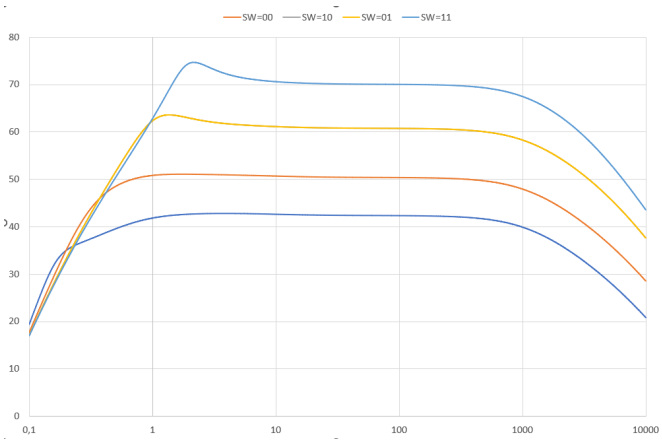

Figure 22. The gain results of each channel of the AFE circuit with AC simulation.

1-channel AFE is also depicted in Figure 25. The assessment results for the 4-channel AFE circuit are displayed in Table III in terms of gain and bandwidth factors.

Each pair of control bits will have different gain coefficients and operating frequency ranges, as shown in Table III. The gain will increase or decrease according to how the bit pair's values are set. The results of the proposed 4-channel AFE circuit are displayed in

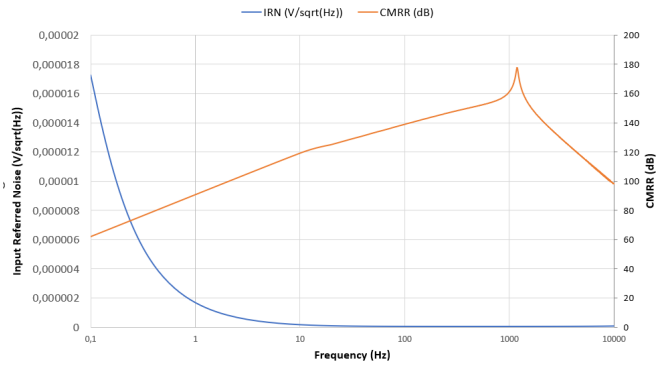

Figure 23. Input-referred noise and CMRR results with AC simulation.

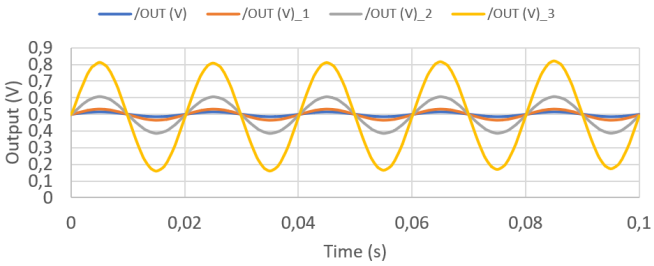

Figure 24. The output amplified signals of the AFE corresponding to SW1-SW2 configuration.

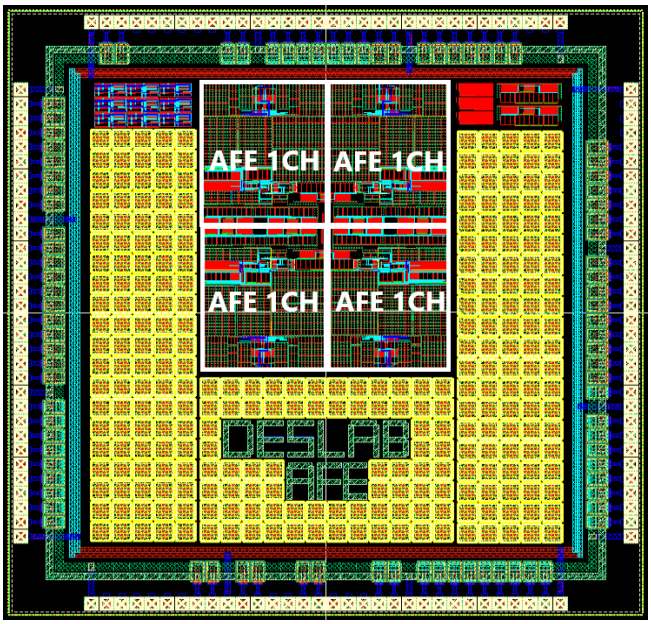

Figure 25. The full-chip layout of the 4-channel AFE on 180nm CMOS process.

Table III
Bandwidth and Gain of the 4-Channel AFE Circuit

Bits (SW1 SW2)	Bandwidth	Gain(dB)
00	0.5 Hz → 2 kHz	42.06
10	0.65 Hz → 1.98 kHz	50.15
01	1.2 Hz → 1.95 kHz	60.5
11	2.3 Hz → 1.8 kHz	70

Table IV
Comparison Results

	[35]	[36]	[37]	[38]	[39]	**This work**
Supply Voltage (V)	0.8	1.2	1.8	1.2	1.8	1
Gain (dB)	60	45.2-71	35.04	26	52-80	**42-70**
Bandwidth	0.9-320 Hz	1 Hz-7 kHz	1 Hz-9.3 kHz	0.1-200 Hz	0.1-100 Hz	**0.5 Hz-2 kHz**
CMRR (dB)	137	>95	76	109.6	>90	**100-180**
IRN (μVrms)	1.7 @100 Hz	2.93	3.2	1.2 @200 Hz	0.91 @100 Hz	**1.8 @1 kHz**
Input Impedance	16-160 GΩ	>100 MΩ	8 MΩ	-	>500 MΩ	**>2 TΩ**
Phase Margin (deg)	-	-	170	-	-	**150-160**
NEF	3.87	3.0	1.94	-	5.1	**1.96**
PEF	11.89	10.8	6.67	-	47	**3.84**
Process (nm)	180	130	180	180	180	**180**

Table IV, along with comparative data with other relevant research. This study has a wider frequency range (from 0.5 Hz to 2 kHz), greater input impedance (>2 TΩ), good phase margin (150-160 deg), higher CMRR (100-180 dB), low IRN (1.8 μVrms at 1 kHz), the lowest NEF/PEF (1.96/3.84), and better gains (42-70 dB) when compared to other research [35–39]. This design has some limitations, including the usage of a large amount of capacitors and the fact that each channel's layout area is roughly 0.35 mm^2.

4 Conclusion

On the 180nm CMOS process, a 4-channel AFE circuit was proposed and simulated. The following blocks are included in the circuit: BCV, CCIA, PGA, and other supported blocks such as Internal Bias and Ring Oscillator. The BCV is proposed to this AFE to configure the electrode's current or voltage input. The AFE's voltage output is suitable for rear analog blocks such as ADCs, filters, and so on. The proposed 4-channel AFE circuit also has high input impedance, low noise, a variety of input signal types, and reconfigurability. The proposed AFE has low noise efficiency with an input-referred noised (IRN) value of 1.8 μVrms, a maximum CMRR of 180 dB, and a high input impedance of greater than 2 TΩ. The circuit can run between 0.5 Hz and 2 kHz to acquire an low EEG bandwidth and record neural signals more efficiently. The circuit operates with a large bandwidth, roughly 2 kHz, which can waste resources, but we have the ability to trade off the magnitude of the bandwidth to reduce the NEF, and PEF coefficients. The suggested AFE can be utilized to capture EEG signals for seizure and epilepsy detection.

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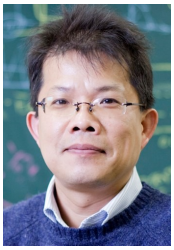

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