Regular Article

FPGA Implementation of Channel Mismatch Calibration in TIADCs for Signals in Any Nyquist Bands

Han Le Duc[1], **Van-Phuc Hoang**[1], **Duc Minh Nguyen**[2]

[1] Le Quy Don Technical University, Hanoi, Vietnam
[2] Hanoi University of Science and Technology, Hanoi, Vietnam

Correspondence: Han Le Duc, email: leduchan@gmail.com
Communication: received 19 September 2017, revised 5 December 2017, accepted 6 December 2017
Online publication: 7 March 2018, Digital Object Identifier: 10.21553/rev-jec.175
The associate editor coordinating the review of this article and recommending it for publication was Dr. Nguyen Truong Khang.

Abstract– **This paper presents a fully digital background calibration technique of the gain and timing mismatches in undersampling Time-Interleaved Analog-to-Digital Converters for the wideband bandlimited input signal at any Nyquist bands. The proposed technique does not require an additional reference channel nor a pilot input. The channel mismatch parameters are estimated based on the mismatch frequency band. The experimental results show the efficiency of the proposed mitigation technique with the SNDR improvement of 16 dB for 4-channel 60 dB SNR TIADC clocked at 2.7 GHz given a multi-tone input occupied at the third Nyquist band. The hardware architecture of the proposed technique is designed and validated on Altera FPGA DE4 board. The synthesized design utilizes a very little amount of the hardware resource in the FPGA chip and works correctly on a Hardware-In-the-Loop emulation framework.**

Keywords– **Gain and timing skews calibration, Undersampling TIADCs, FPGA implementation, Nyquist Zones.**

1 Introduction

In the direct-sampling next-generation receivers, an Analog to Digital Converters (ADC) is put as close as possible to the antenna, hence, they play very important role. Such ADCs need to support very high sampling rates with high resolution and low-power dissipation. A Time-interleaved ADC (TIADC) which is constructed by two or more slow but accurate ADCs in parallel, is a promising solution to achieve these goals [1, 2]. Unfortunately, the drawbacks of such time-interleaved architecture are the channel mismatches among individual ADCs including offset, gain and timing mismatches. These channel mismatches significantly degrade the performance of the TIADC, limiting the possibilities of employing this technique [3]. Thus, calibration techniques are usually applied in TIADC to reduce the distortion errors due to the channel mismatches. In this framework, we focus on mitigating errors due to gain and timing mismatches since the offset mismatch is the static error, which is easier to correct [4]. Moreover, the impact of timing mismatches increase with the input frequency that overshadows other nonidealities in TIADC for broadband inputs [2].

Analog and/or mixed signal calibration techniques proposed in [5–7] exhibit good performance. However, the analog correction schemes limit the overall ADC resolution due to variations in process, supply voltage and temperature as well as thermal noise. Moreover, they require additional development time and are not portable between CMOS technology nodes. Thanks to technology node shrinking, all-digital techniques [3, 8–18] are the promising solution to eliminate the issues of the analog and mixed-signal calibration. The all digital calibration techniques can be developed faster, able to exploit advantages of CMOS technology scaling, and easier to port to the next technology generation [19]. Most of them [3, 8–14], are derived with an assumption that the input signal is band-limited to the Nyquist frequency, i.e., the input located at the first *Nyquist Band (NB)*, also commonly known as *Nyquist Zone (NZ)*. However, these techniques is not directly applied for the undersampling (or subsampling) TIADCs which samples the band-limited signals in the higher NBs. The undersampling technique is a promising solution in next-generation direct-sampling receivers such as subsampling receivers, software defined radios, and broadband satellite receivers [18, 20]. Recently, all-digital calibration techniques of the channel mismatches in TIADCs for the input at any NBs, has been proposed in [15–19]. The calibration technique in [16] requires an additional channel and the channel mitigation technique in [17] uses a pilot input signal. The work in [15] is performed with the assumption of narrow-band signals and applied for only two channels. In order to estimate the channel mismatch parameters, the approaches proposed in [18, 19] effectively force the zero-crosscorrelation between two adjacent sub-ADC outputs or between the compensated TIADC output and the error signals due to the channel mismatches. They are heavily relied on the statistics of the input signal.

Leveraging the channel mismatch mitigation techniques proposed in [3], we extend the gain and timing mismatch calibration proposed in [3] to the input signal

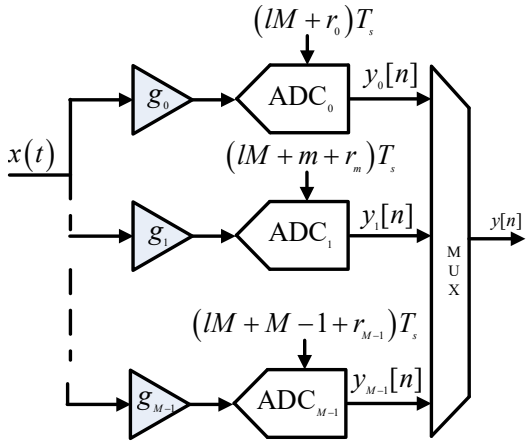

Figure 1. An M-channel TIADC with gain and timing mismatches.

at any NZs. The proposed technique uses the mismatch band based estimation and relaxes requirements for the input signal statistics. In addition, we design and validate the proposed mechanism on a field-programmable gate array (FPGA) platform.

The rest of the paper is organized as follows. Section 2 analyses the impact of the gain and timing mismatches on the TIADC performance. Section 3 is dedicated to propose the gain and timing mitigation technique in the TIADC for input located at any NBs. Section 4 presents the optimal hardware architecture to validate the proposed technique on the FPGA platform. Section 5 shows the experimental results. Finally, the conclusion and future direction are given in Section 6.

2 Time-interleaved Analog to Digital Converters

Figure 1 shows the block diagram of an M-channel TIADC with gain and timing mismatches. g_m and $r_m T_s$ denote the gain and timing mismatches in the m^{th}-channel, where r_m presents the relative timing mismatch and T_s is the overall sampling period. The input signal $x(t)$ is fed into each channel where it is multiplied by g_m and then is sampled at instant time of $(lM+m)Ts + r_m T_s$, generating a sequence $y_m[l]$. The data streams $y_m[l]$ from all channels are combined by a multiplexer (MUX) to generate an output sequence $y[n]$. As a result, the effective sampling period of $y[n]$ is T_s.

We assume a slightly oversampled and bandlimited input $x(t)$, i.e., $X(j\Omega) = 0$ for $|\Omega T_s| \geq \pi$ that is a realistic model for some communication signals as presented in software defined radios. The discrete-time Fourier transform (DFT) of the output $y[n]$ can be expressed as [3, 21]

$$Y\left(e^{j\omega}\right) = \sum_{k=0}^{M-1} X\left(e^{j(\omega-\frac{2\pi k}{M})}\right) \breve{H}_k\left(e^{j(\omega-\frac{2\pi k}{M})}\right), \quad (1)$$

where $X\left(e^{j\omega}\right)$ is the discrete-time spectrum of the sampled input $x[n] = x(t)|_{t=nT_s}$ and

$$\begin{aligned} \breve{H}_k(e^{j\omega}) &= \tfrac{1}{M}\sum_{m=0}^{M-1} g_m e^{r_m H_d(e^{j\omega})} e^{-jk\frac{2\pi}{M}m}, \\ H_d\left(e^{j\omega}\right) &= j\omega, \text{for} -\pi < \omega < \pi, \end{aligned} \quad (2)$$

where $H_d\left(e^{j\omega}\right)$ is the frequency response of an ideal derivative filter [22].

Obviously from (1), if the TIADC has channel mismatches, the output spectrum consists of the original spectrum $X\left(e^{j\omega}\right)$ multiplied by $\breve{H}_0\left(e^{j\omega}\right)$, and frequency-shifted versions of the products $X\left(e^{j\omega}\right)\breve{H}_k\left(e^{j\omega}\right)$ as shown in Figure 2. The frequency-shifted products are referred to as the errors due to channel mismatches that need to be mitigated.

3 Proposed Calibration Technique for Signals in any Nyquist Zone

3.1 Digital Correction

Assuming the clock skews r_m are small, exploiting the Taylor's series approximation, and neglecting the high order components, we have

$$e^{jr_m H_d(e^{j\omega})} \approx 1 + r_m H_d(e^{j\omega}). \quad (3)$$

Replacing (2) into (3) gives

$$\breve{H}_k(e^{j\omega}) = G_k + R_k H_d\left(e^{j\omega}\right), \quad (4)$$

where

$$\begin{aligned} G_k &= \tfrac{1}{M}\sum_{m=0}^{M-1} g_m e^{-jk\frac{2\pi}{M}m}, \\ R_k &= \tfrac{1}{M}\sum_{m=0}^{M-1} g_m r_m e^{-jk\frac{2\pi}{M}m}. \end{aligned} \quad (5)$$

Note that the information about the gain and timing mismatches across the individual channels is contained in the variables $\{G_k, R_k\}$. Without loss of generality, it can be assumed that the average value of the timing mismatches is zero, i.e., $R_0 \approx 0$ or can be neglected [3]. Apparently, G_0 represents the average gain mismatch across all channels. In order to be ease of notation, we assume $G_0 = 1$, otherwise the compensated signals will be $G_0 x[n]$. The inverse DFT of (1) can be written as [3]

$$y[n] = x[n] + e[n], \quad (6)$$

where $e[n]$ is the error due to the gain and timing mismatches. It can be expressed as the sum of two inner-product components:

$$e[n] = c_g^T \mathbf{x}_{g,n} + c_r^T \mathbf{x}_{r,n}, \quad (7)$$

where signal vectors are defined as

$$\begin{aligned} \mathbf{x}_{g,n} &= \mathbf{m}_n x[n], \\ \mathbf{x}_{r,n} &= \mathbf{m}_n \left(h_d[n] * x[n]\right). \end{aligned} \quad (8)$$

$h_d[n]$ is the impulse response of the ideal derivative filter. The modulation vector $\mathbf{m}_n$ is expressed as

$$\begin{aligned} \mathbf{m}_n = \Big(&2\cos\left(1\tfrac{2\pi}{M}n\right), -2\sin\left(1\tfrac{2\pi}{M}n\right), \ldots, \\ &2\cos\left(k\tfrac{2\pi}{M}n\right), -2\sin\left(k\tfrac{2\pi}{M}n\right), \ldots, \\ &2\cos\left(\left(\tfrac{M}{2}-1\right)\tfrac{2\pi}{M}n\right), -2\sin\left(\left(\tfrac{M}{2}-1\right)\tfrac{2\pi}{M}n\right), (-1)^n\Big)^T, \end{aligned} \quad (9)$$

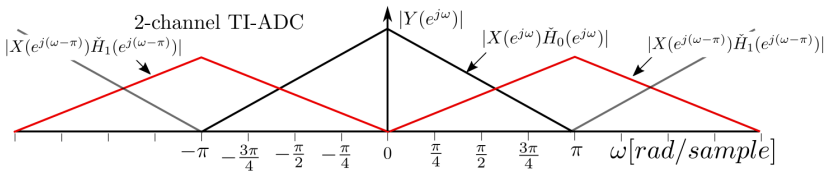

Figure 2. The Spectrum of the TIADC output for $M = 2$.

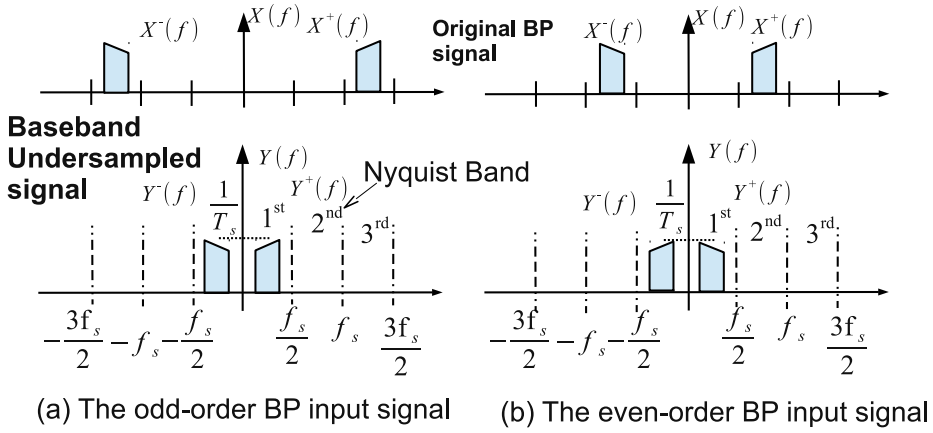

Figure 3. Undersampling Process in an undersampling TIADC.

where T notates the matrix transpose operator. The gain and timing mismatch coefficient vectors of c_g, c_r are defined by

$$c_g = \Big(Re\{G_1\}, Im\{G_1\}, \ldots, Re\{G_{\frac{M}{2}-1}\}, Im\{G_{\frac{M}{2}-1}\}, (-1)^n\Big)^T, \quad (10)$$

$$c_r = \Big(Im\{R_1\}, Im\{R_1\}, \ldots, Re\{R_{\frac{M}{2}-1}\}, Im\{R_{\frac{M}{2}-1}\}, (-1)^n\Big)^T. \quad (11)$$

From (7) and (8), the input derivative is required to recover the error signal due to the gain error and timing skew. This derivative is computed by a fixed ideal differentiator filter $h_d[n]$.

Regarding Bandpass (BP) RF input at higher NBs, TIADC processes an analog input signal located above the first NB (1st NB frequency range: $\left[0; \frac{f_s}{2}\right]$). The analog BP input signal is passed through an TIADC to generate the output data stream. The BP sampling process folds the input signal back to the first NB (or baseband) as illustrated in the Figure 3. Obviously, the odd-order bandpass sampling makes the base-band spectra the same as the original spectrum as shown in Figure 3(a). For even-order undersampling process, the base-band frequency spectra is inverse to the original input spectrum as described in Figure 3(b). Thus, the derivative filter $h_d[n]$ needs to be re-designed in the channel mismatch calibration for input at higher NBs. Considering a bandpass input signal located at k_{NB}-th Nyquist band, its first order derivative is expressed as [23]

$$x'[n] = y'[n] + (-1)^k_{NB} \left\lfloor \frac{k_{NB}}{2} \right\rfloor 2\pi\hat{y}[n], \quad (12)$$

where $\hat{y}[n]$ is the Hilbert transform of $y[n]$. From (12), a filter consisting of the base-band derivative filter $h_d[n]$, a FIR Hilbert filter and a scaling factor of $(-1)^k_{NB} \left\lfloor \frac{k_{NB}}{2} \right\rfloor 2\pi$, is used to calculate the derivative of input at any NBs. Physically, an additional Hilbert transformer is an all-pass filter that shifts the input signal phase by 90^0 [22]. It covers the bandwidth of the signal to be phase shifted as illustrated in the even-order bandpass sampling.

To correct the channel mismatches, the error signal in (7) and signal vectors in (8) need to be determined. These signals are the functions of input signal. However, in blind calibration, the input is unknown and the output is thus used instead of input for approximation. From (7), (8) and (12), the estimate of $e[n]$ is therefore expressed as

$$\hat{e}[n] = \hat{c}_g^T \underbrace{\mathbf{m}_n y[n]}_{\hat{\mathbf{x}}_{g,n}} + \hat{c}_r^T \underbrace{\mathbf{m}_n \Big(h_{bpd}[n] * y[n]\Big)}_{\hat{\mathbf{x}}_{r,n}}, \quad (13)$$

where $h_{bpd}[n]$ is defined to be a impluse response of the bandpass derivative filter presenting the transfer function of (12). From (12), $h_{bpd}[n]$ is expressed as

$$h_{bpd}[n] = h_d[n] + (-1)^{k_{NB}} \left\lfloor \frac{k_{NB}}{2} \right\rfloor 2\pi h_h[n]. \quad (14)$$

$h_h[n]$ is a impulse response of the Hilbert filter. $\hat{c}_g^T$ and $\hat{c}_r^T$ are estimates of the vectors c_g^T and c_r^T, respectively. Using (6), then

$$x[n] \approx y[n] - \hat{e}[n]. \quad (15)$$

Finally, the proposed digital correction technique is shown in Figure 4. This technique can be extended to arbitrary number of channels in the time-interleaving architecture.

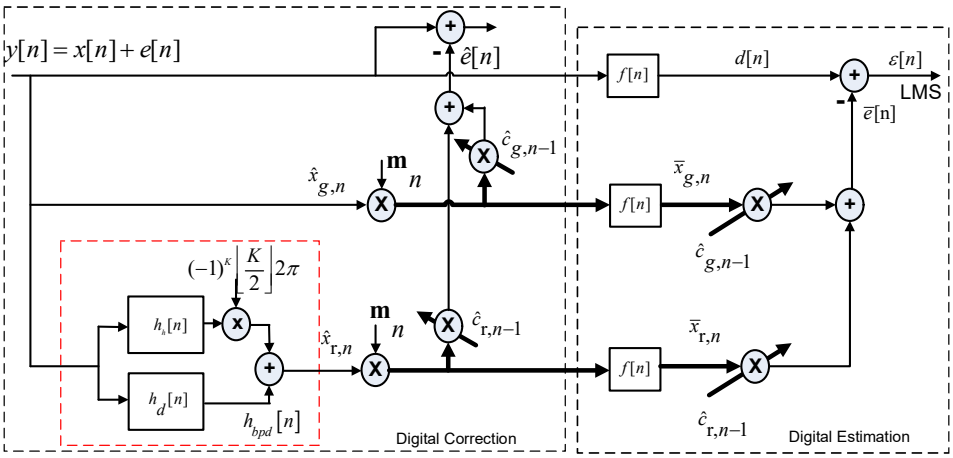

Figure 4. All-digital gain and timing mismatch mitigation technique for input at any NB.

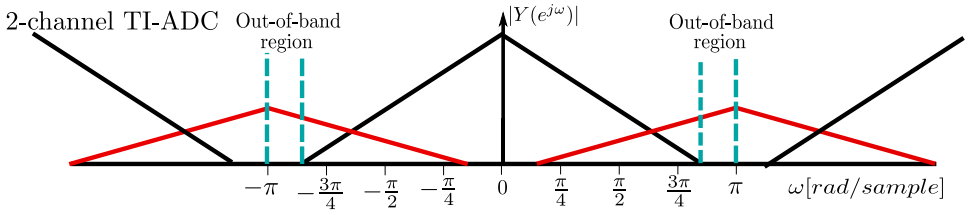

Figure 5. The Spectrum of the TIADC output for $M = 2$ with the present of out-of-ban region (or mismatch band).

3.2 Digital Estimation

In order to estimate the vectors $\{c_g, c_r\}$, Vogel *et al.* in [3] assumes that the input signal is a bandlimited low-pass signal and that the TIADC oversamples the input. Oversampling produces a higher frequency band so-called mismatch band that is free of signal content. This frequency band will only contain the energy of image signals that arise from the error spectra due to the gain and timing mismatches as shown in Figure 5. Thus, the out-of-band region (or mismatch band) contains only error spectra. Minimizing the error signals in this mismatch band by LMS algorithm is to estimate the gain and timing mismatch coefficients $\{c_g, c_r\}$. The filters $f[n]$ diminish the input signal energy and pass only the image energy in the mismatch band. The estimated vectors $\hat{\mathbf{x}}_{g,n}$ and $\hat{\mathbf{x}}_{r,n}$ are also filtered through $f[n]$ to generate $\{\bar{\mathbf{x}}_{g,n}, \bar{\mathbf{x}}_{r,n}\}$. The LMS algorithm [24] is used to minimize the error signal $\varepsilon[n] = d[n] - \bar{e}[n]$ in order to estimate the channel mismatch coefficients. The coefficients of (10) and (11) can be derived from the updating equations by the adaptive LMS algorithm as [3]

$$\begin{aligned} \hat{c}_{g,n} &= \hat{c}_{g,n-1} + \mu_g \bar{\mathbf{x}}_{g,n}^T \varepsilon[n], \\ \hat{c}_{r,n} &= \hat{c}_{r,n-1} + \mu_r \bar{\mathbf{x}}_{r,n}^T \varepsilon[n], \end{aligned} \tag{16}$$

where μ_g and μ_r are the step size parameters of LMS algorithms for gain and timing mismatches, respectively. It would be worth noting that the channel mismatch coefficients are updated by an amount being cross-product of two error signals (the channel mismatch induced image signals and their estimates), hence relaxing the requirements of the input statistical properties [5, 25].

4 The Proposed Optimal Hardware Architecture

FPGA implementation using Matlab/Simulink in [23] is applied in this framework. The hardware architecture of the proposed calibration is designed and optimized in terms of fixed-point representation of signals that is characterized by signal ranges and signal *Word-Length* (WL). So the parameters of the Optimal Fixed-point Simulink (OFpS) model that need to be optimized, are the order of FIR filters and the signal WLs. The signal ranges of block signals in the OFpS model are mathematically computed based on the transfer function of DSP blocks and simulations as done in [23]. The signal ranges and signal WLs would determine the fractional bits (or precision) used to convert signal values into a binary representation.

The OFpS model (or hardware architecture) processes real-time signal data in sample-by-sample manner. Therefore, the delays of each signal datapath are made balanced. Note that, pipeline registers are inserted to reduce the combinational path length and improve the global working frequency and throughput [18]. Figure 6 shows the pipelined OFpS architecture of the proposed calibration. z^{-k} blocks are delayed/pipeline registers. The notation of sfix13_En11 presents a 13-bit signed fixed-point data type with a Fraction Length (FL) or fractional bits of 11, i.e., WL = 13 bits and FL = 11 bits. Generally, the representable fixed-point number is actually bounded by $(-2^{\mathrm{WL}-1-\mathrm{FL}}, (2^{\mathrm{WL}-1}-1)2^{-\mathrm{FL}})$. The LMS block in the proposed hardware architecture presents simply the adaptive LMS algorithms expressed in (16). The TIADC outputs are represented on 13 bits

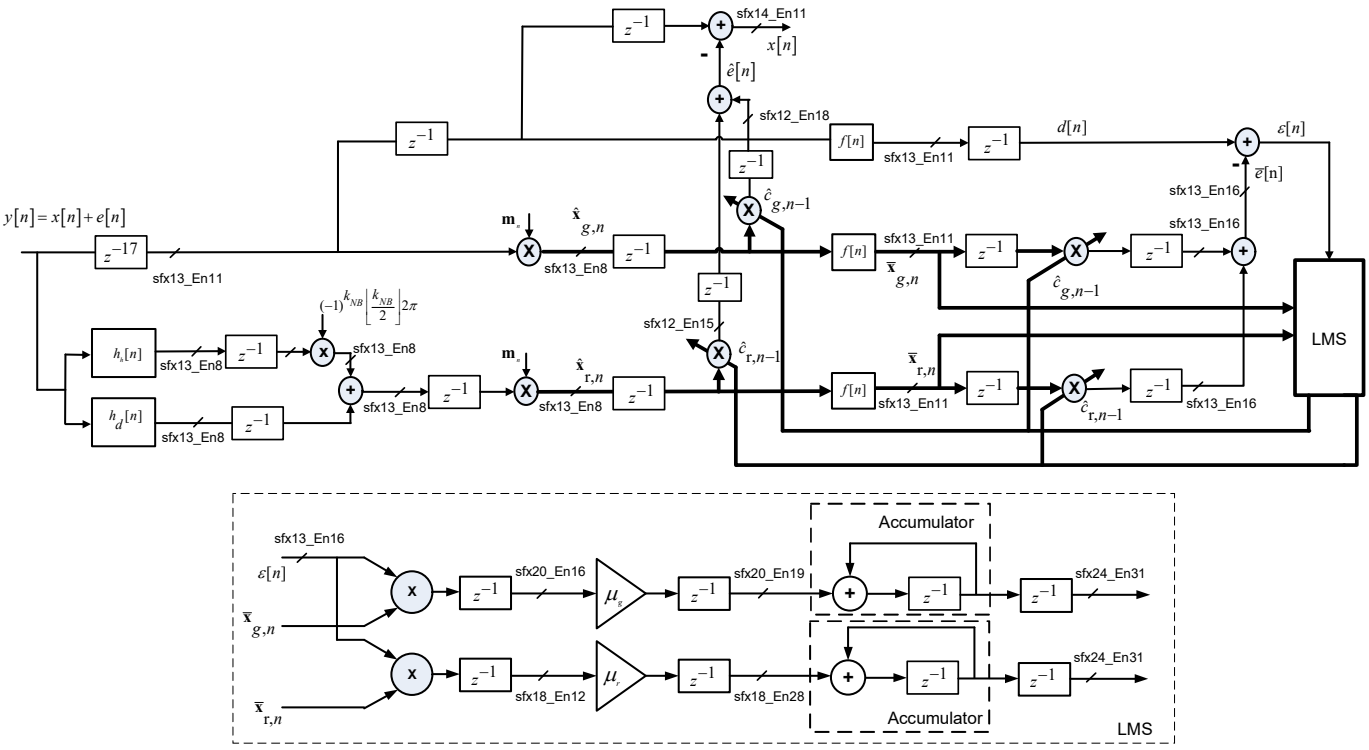

Figure 6. Hardware Implementation Architecture.

to decrease the sensitivity to digital truncation errors. System-level simulations reveal that the corrected compensated outputs are presented by 14 bits for minimum digital truncation errors. Both the ideal differentiator and Hilbert filter are designed with the optimal FIR order of 30. As shown in Figure 6, the latency between the distorted output and the compensated output is 19 clock cycles.

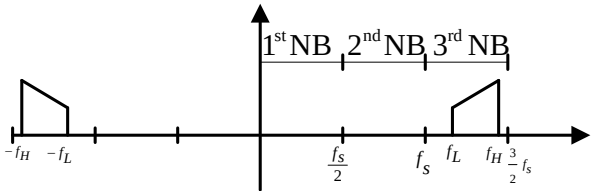

Figure 7. Nyquist Band (or Nyquist zone) definition.

5 Experimental Results

5.1 Simulation Results

To verify the efficiency of the proposed technique, simulations are carried out on a four-channel TIADCs with 60 dB SNR (thermal noise level) clocked at $f_s = 2.7$ GHz. Both the ideal differentiator and Hilbert filters have 31 taps. The coefficients of FIR filters are obtained by multiplying the exact coefficients with a Hanning window. Filters $f[n]$ are designed using *fdesign* function of Matlab where the number of taps is 31 and the cut-off frequency is 0.8π. The channel mismatches are Gaussian with zero mean and standard deviation of 0.33 ps for timing errors and 0.2% for gain error. The step size parameters of μ_g and μ_r are chosen by using simulation in order to achieve a good compromise between the convergence speed and the parameter estimation precision [24]. Moreover, the adaptive parameters are chosen to be the power of two since the multiplication with power of 2 is optimally executed by binary shifters, leading to optimize hardware architecture and to reduce hardware cost. In our simulation and hardware implementation, the iteration step size parameters of μ_g and μ_r are respectively selected to be 2^{-5} and 2^{-7}.

We simulated with 42-tone bandpass sinusoid input with $f_L = 3.24$ GHz and $f_H = 3.78$ GHz as illustrated in Figure 7. This bandpass input signal is occupied in the third NB. Undersampling TIADC directly down-converts the bandpass input to the frequency baseband $(0, \frac{f_s}{2}) = (0, 1.3\text{ GHz})$, i.e., f_L and f_H map to 540 MHz and 1.08 GHz, respectively as illustrated in Figure 8. The overall performance of the proposed calibration has been evaluated based on the signal-to-noise-distortion (SNDR) ratio for the uncorrelated output given by [3]

$$\text{SNDR} = 10\log_{10}\left(\frac{\sum_{n=0}^{N-1}|x[n]|^2}{\sum_{n=0}^{N-1}|x[n]-y[n]|^2}\right), \qquad (17)$$

and for the calibrated output given by [3]

$$\text{SNDR} = 10\log_{10}\left(\frac{\sum_{n=0}^{N-1}|x[n]|^2}{\sum_{n=0}^{N-1}|x[n]-\hat{y}[n]|^2}\right), \qquad (18)$$

where $y[n], \hat{y}[n]$ are the distorted output and compensated output of TIADC before and after calibration. $x[n]$ is the input of TIADC. The uncalibrated and calibrated output spectra are presented in Figure 8(a) and (b), respectively. It can be seen that the distortions of in-band and out-of-ban regions due to gain and timing skews,

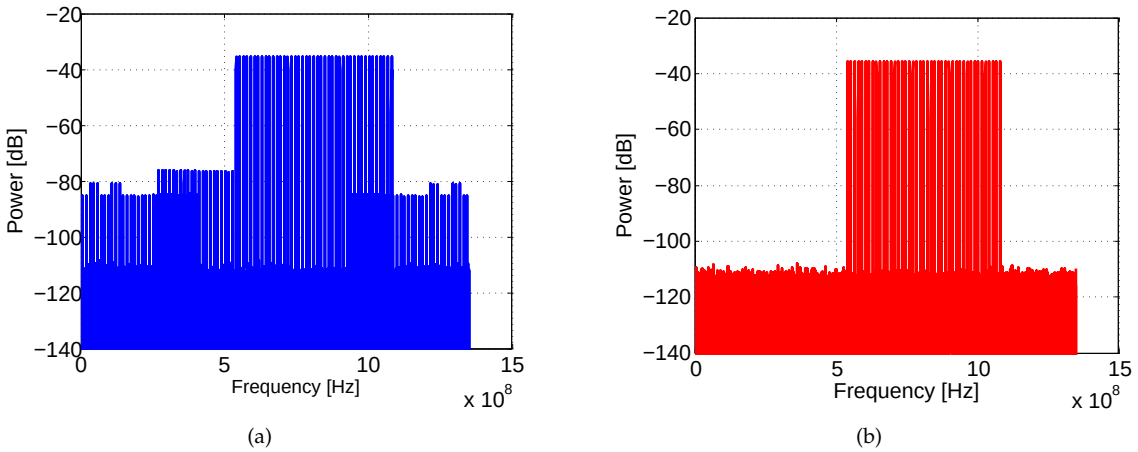

Figure 8. Output spectra for BP input signal with $f_L = 3.24$ GHz, $f_H = 3.24$ GHz in the third NB and $f_s = 2.7$ GHz: (a) before calibration: SNDR = 42.37 dB and (b) after calibration: SNDR = 58.45 dB (cutoff frequencies of f_L, f_H map to 540 MHz and 1.08 GHz in baseband, respectively).

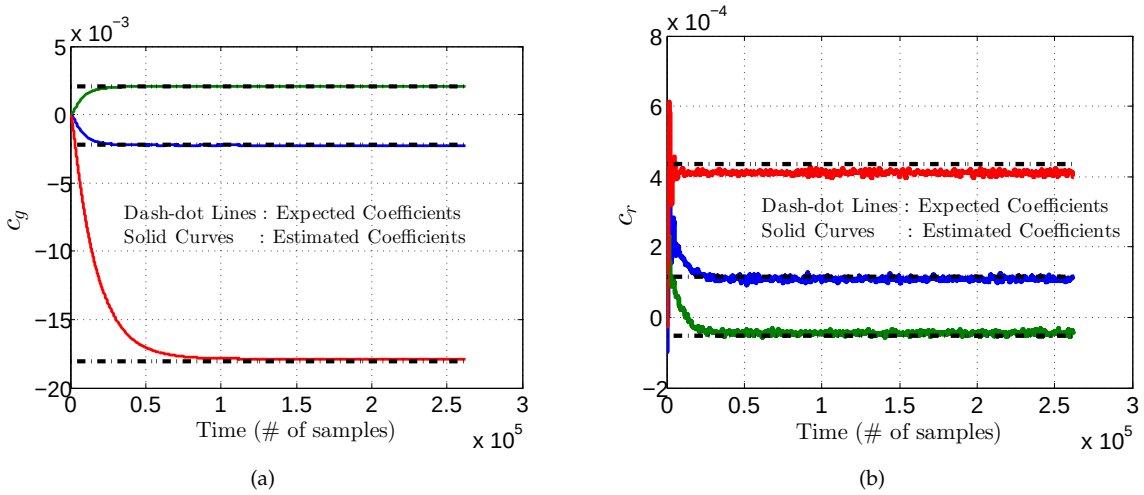

Figure 9. Convergence behavior: (a) gain parameters and (b) timing parameters.

reduce to the noise floor. The proposed technique obtains the SNDR improvement of approximately 16 dB.

The convergence behaviour of the gain and timing coefficients is shown in Figure 9(a) and (b), respectively. The parameter estimates (solid curves) have settled to their expected values (dash-dot lines) after approximately 50K-samples (or 18.5 μs).

5.2 Hardware Validation

The OFpS model is converted into Hardware Description Language (HDL) using Matlab HDL Coder toolbox. In this framework, Verilog code is generated automatically for the FPGA implementation. The Hardware-In-Loop (HIL) emulation methodology in [23] is applied to validate the proposed calibration on an Altera FPGA board. HIL emulation allows access to real hardware in a simulation and adds an HIL block into the Simulink model in order to cosimulate the register-transfer level (RTL) design with a physical FPGA board implementing portions of that design [4]. The HDL design is systhesized and loaded into Altera FPGA DE4 board which houses the Altera Stratix IV FPGA chip EP4SGX230KF40C2. The design executed in the FPGA board together with the Simulink model in PC.

Table I
FPGA Synthesis Results

Family	Stratix IV
Device	EP4SGX230KF40C2
Logic utilization	5%
Combinational ALUTs	7,391 / 182,400 (4%)
Memory ALUTs	28 / 91,200 (< 1%)
Dedicated logic registers	7,743 / 182,400 (4%)
Total registers	14743
DSP block 18-bit elements	24 / 1,288 (2%)
Fmax	205.35 MHz

The Simulink model acts as the testbench environment providing the design on the FPGA with inputs and displaying the output of the design. As shown in Table I, the synthesized circuit operates properly on the FPGA at the clock frequency of 205 MHz and consumes very little hardware resources of the FPGA chip. As a matter of fact, the fixed-point coding, optimization of the filter coefficients and the signal path Word-Length (WL) were performed using Matlab-Simulink. Using this study, the outputs of the proposed hardware architecture are iden-

tical to those of the floating-point simulink model. As a consequence, the gain and timing mismatch coefficients of the proposed hardware architecture also converges to their expected values after 50 K-samples (or 18.5 μs) as presented in Figure 9.

6 Conclusion

This paper presents the all-digital background calibration technique of the gain and timing mismatches in TIADC for input at any NBs. The proposed technique does not require an additional reference channel nor a pilot input. It is the adaptive calibration tracking the gain and timing mismatch fluctuation due to temperature, voltage and aging variation. It requires the slightly oversampled input signals, leading the exist of the free-band where there is only the spurs due to mismatches. Minimizing the errors in the free-band using LMS algorithms, the channel mismatch coefficients are updated by an amount being cross-product of two error signals (the channel mismatch induced image signals and their estimates), hence relaxing the requirements of the input statistical properties. It is worth noting that the slightly oversampled input signal is one of the realistic models for some next-generation communication signals. As a result, the proposed calibration can be applied to next-generation communication systems such as subsampling receivers, software defined radios, and broadband satellite receivers. The simulation results shows the efficiency of the proposed calibration leading to SNDR improvement of 16 dB for 4-channel 60 dB SNR TIADC clocked at 2.7 GHz with the multi-tone input occupied at the third NB. The optimal hardware architecture of the proposed technique is developed and correctly validated on the Altera FPGA DE4 board which houses the Altera Stratix IV FPGA chip EP4SGX230KF40C2. The latency between the distorted output and the compensated output of the tested TIADC is 19 clock cycles (or 0.007 μs). The synthesized result shows that the digital circuit operates properly on the FPGA and utilizes a small amount of hardware resources of the FPGA chip. The proposed hardware architecture converges after 50 K-samples (or 18.5 μs). The further optimized ASIC implementation and comparison with the state-of-the-art techniques are underway.

Acknowledgment

This research is funded by Vietnam National Foundation for Science and Technology Development (NAFOSTED) under grant number 102.02-2016.12.

References

[1] J. Black, W.C. and D. Hodges, "Time interleaved converter arrays," *IEEE Journal of Solid-State Circuits*, vol. 15, no. 6, pp. 1022–1029, Dec. 1980.

[2] B. Razavi, "Design Considerations for Interleaved ADCs," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1806–1817, 2013.

[3] C. Vogel, S. Saleem, and S. Mendel, "Adaptive blind compensation of gain and timing mismatches in M-channel time-interleaved ADCs," in *Proceedings of the 15th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2008)*, 2008, pp. 49–52.

[4] H. Le Duc, "All-digital Calibration Techniques of Timing Skews for Undersampling Time-Interleaved ADCs," Ph.D. dissertation, COMELEC Department, Telecom-ParisTech, 46 Rue Barrault, 75013 Paris, Dec. 2015.

[5] D. Stepanovic and B. Nikolic, "A 2.8 GS/s 44.6 mW Time-Interleaved ADC Achieving 50.9 dB SNDR and 3 dB Effective Resolution Bandwidth of 1.5 GHz in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 4, pp. 971–982, Apr. 2013.

[6] M. El-Chammas and B. Murmann, "A 12-GS/s 81-mW 5-bit time-interleaved flash ADC with background timing skew calibration," in *Proceedings of the IEEE Symposium on VLSI Circuits (VLSIC)*, Jun. 2010, pp. 157–158.

[7] D. Camarero, K. Ben Kalaia, J.-F. Naviner, and P. Loumeau, "Mixed-Signal Clock-Skew Calibration Technique for Time-Interleaved ADCs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 11, pp. 3676–3687, 2008.

[8] N. Le Dortz, J.-P. Blanc, T. Simon, S. Verhaeren, E. Rouat, P. Urard, S. Le Tual, D. Goguet, C. Lelandais-Perrault, and P. Benabes, "22.5 A 1.62GS/s time-interleaved SAR ADC with digital background mismatch calibration achieving interleaving spurs below 70dBFS," in *Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2014, pp. 386–388.

[9] J. Matsuno, T. Yamaji, M. Furuta, and T. Itakura, "All-Digital Background Calibration Technique for Time-Interleaved ADC Using Pseudo Aliasing Signal," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1113–1121, 2013.

[10] P. Satarzadeh, B. Levy, and P. Hurst, "A parametric polyphase domain approach to blind calibration of timing mismatches for M-channel time-interleaved ADCs," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2010, pp. 4053–4056.

[11] V. Divi and G. W. Wornell, "Blind Calibration of Timing Skew in Time-Interleaved Analog-to-Digital Converters," *IEEE Journal of Selected Topics in Signal Processing*, vol. 3, no. 3, pp. 509–522, 2009.

[12] S. Huang and B. Levy, "Blind Calibration of Timing Offsets for Four-Channel Time-Interleaved ADCs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 4, pp. 863–876, Apr. 2007.

[13] T. Oshima, T. Takahashi, and T. Yamawaki, "Lms calibration of sampling timing for time-interleaved a/d converters," *Electronics Letters*, vol. 45, no. 12, pp. 615–617, Jun. 2009.

[14] J. A. McNeill, C. David, M. Coln, and R. Croughwell, "'Split ADC' Calibration for All-Digital Correction of Time-Interleaved ADC Errors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 5, pp. 344–348, May 2009.

[15] S. Jamal, D. Fu, M. Singh, P. Hurst, and S. Lewis, "Calibration of Sample-Time Error in a Two-Channel Time-Interleaved Analog-to-Digital Converter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 4, pp. 822–822, 2005.

[16] F. Centurelli, P. Monsurro, and A. Trifiletti, "Efficient Digital Background Calibration of Time-Interleaved Pipeline Analog-to-Digital Converters," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 59, no. 7, pp. 1373–1383, 2012.

[17] F. Harris, X. Chen, E. Venosa, and F. A. N. Palmieri, "Two channel TI-ADC for communication signals," in *Proceedings of the IEEE 12th International Workshop on Signal Processing Advances in Wireless Communications*, Jun. 2011, pp. 576–580.

[18] H. Le Duc, D. M. Nguyen, C. Jabbour, T. Graba, P. Des-

greys, O. Jamin, and V. T. Nguyen, "All-Digital Calibration of Timing Skews for TIADCs Using the Polyphase Decomposition," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 1, pp. 99–103, Jan. 2016.

[19] H. Le Duc, D. M. Nguyen, C. Jabbour, P. Desgreys, O. Jamin, and V. T. Nguyen, "Fully Digital Feedforward Background Calibration of Clock Skews for Sub-Sampling TIADCs Using the Polyphase Decomposition," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 6, pp. 1515–1528, Jun. 2017.

[20] S. Louwsma, E. van Tuijl, M. Vertregt, and B. Nauta, "A Time-Interleaved Track & Hold in 0.13μm CMOS sub-sampling a 4 GHz signal with 43 dB SNDR," in *Proceedings of the Custom Integrated Circuits Conference (CICC '07)*. IEEE, Sep. 2007, pp. 329–332.

[21] C. Vogel, "The Impact of Combined Channel Mismatch Effects in Time-Interleaved ADCs," *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 1, Feb. 2005.

[22] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing: Principles, Algorithms and Applications.* Upper Saddle River, New Jersey, 2007.

[23] H. Le Duc, D. M. Nguyen, C. Jabbour, T. Graba, P. Desgreys, O. Jamin, and V. T. Nguyen, "Hardware Implementation of All Digital Calibration for Undersampling TIADCs," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 2181–2184.

[24] P. Diniz, *Adaptive Filtering: Algorithms and Practical Implementation*, ser. Kluwer international series in engineering and computer science. Springer, 2008.

[25] H. Le Duc, C. Jabbour, P. Desgreys, and V. T. Nguyen, "Estimation Techniques for Timing Mismatch in Time-interleaved Analog-to-Digital Converters: Limitations and solutions," in *Proceedings of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Dec. 2016, pp. 297–300.

Han Le Duc received the Ph.D. degree in Electronics and Communications from the Institute Mines Telecom (Telecom Paristech), Paris, France in 2015 and the M.Sc. degree in Communication Engineering from RWTH Aachen University, at Aachen, Germany in 2012. He is working as scientific researcher in Faculty of Radio-Electronic Engineering, Le Quy Don Technical University, Hanoi, Vietnam. In 2016, he worked at the Institute Mines Telecom as a postdoc researcher.

His main research interests include digital IC design, advanced digital signal processing algorithms for communication systems, linearization of non-linear wireless communication systems (wideband RF transceivers for 4G/5G wireless communication), digital predistortion for RF power amplifier and the channel mismatch calibration in time-interleaved ADCs.

Van-Phuc Hoang was born in Hung Yen, Vietnam. He received Ph.D. degree in Electronic Engineering from the University of Electro-Communications, Tokyo, Japan in 2012. He is working as Deputy Head of The Department of Microelectronics, Le Quy Don Technical University, Hanoi, Vietnam. His research interests include digital circuits and systems, low power IC design, hardware security, embedded systems and VLSI architecture for digital signal processing.

Duc Minh Nguyen received the M.Sc. and Ph.D. degree in electrical engineering from University of Kaiserslautern, Germany, in 2009. He worked as a Scientific Staff Member at University of Kaiserslautern from 2003 until 2010. In 2014, he is postdoctoral researcher at the Institut Mines-Telecom, France. In 2016, he became an Associate Professor at Hanoi University of Science and Technology, Vietnam. His research activities involve digital hardware design, embedded system design, formal modeling and verification of digital design and embedded systems.